DESIGN VARIATIONS FOR SUPPRESSING LATCH-UP IN CMOS CIRCUITS STUDIED BY 2-D TRANSIENT DEVICE SIMULATION

H.Jacobs, R.Kircher, C.Werner, M.Strzempa-Depré, K.-P.Karmann

Siemens AG
Central Research and Development, Microelectronics,
Otto-Hahn-Ring 6, D-8000 Munich 83, FRG

SUMMARY

The latch-up sensitivity of VLSI CMOS circuits can be drastically reduced by using an epitaxial layer on top of a highly doped substrate. A less expensive design measure is to implement properly placed well and substrate contacts (guard rings), thus reducing the shunt resistances which are decisive for the forward biasing of the parasitic bipolar transistors.
In this work, 2-D transient device simulation is used to compare these design variations with respect to their effects on latch-up hardness.

1. INTRODUCTION

The latch-up effect in CMOS devices, the firing of parasitic SCR's, imposes severe constraints on further miniaturization of CMOS VLSI circuits. Consequently, the latch-up phenomenon has been subject to intense investigation. Besides full 2-D numerical simulations of the latch-up path /1-6/, design tools have been developed basing on simplified analytical models /1, 4, 7/. The simulations have been concentrating mostly on standard CMOS structures without any design modifications for latch-up suppression.
The purpose of the present work was to gain physical insight into the mechanisms of transient latch-up triggering when an epitaxial layer or guard rings are used for latch-up protection.
We have utilized the 2-D transient device simulation program BAMBI /8/ to simulate overvoltage transients at the source/drain regions of a typical n-well CMOS structure.

2. DEVICE STRUCTURE

Schematic cross sections of the simulated latch-up test structures are shown in Fig. 1 for a structure with (Fig.1a) and without guard rings (Fig.1b). A structure similar to Fig.1b was simulated to study the influence of an epitaxial layer. The test structures contain n and p source/drain regions as well as surface contacts to the well and to the substrate.
Typical device dimensions are given in Table 1. All structures were fabricated with a 2.5 μm deep n-well. The substrate resistivity was 10 Ω cm for all structures without epitaxial layer.
A 10 Ω cm epitaxial layer of 8 μm thickness on a 0.01 Ω cm substrate was used in these studies.

Table 1: Typical device dimensions

	with guard rings	w/o guard rings	with epi layer
n/p emitter spacing	14 μm	7.2 μm	12.0 μm
p contact/ n emitter spacing	2 μm	2 μm	20 μm
n contact/ p emitter spacing	2 μm	2 μm	40 μm

The doping profiles for input into BAMBI were extracted from 1-D SUPREM II /9/ simulations. The underdiffusion phenomenon was accounted for by radius functions at the mask edges.

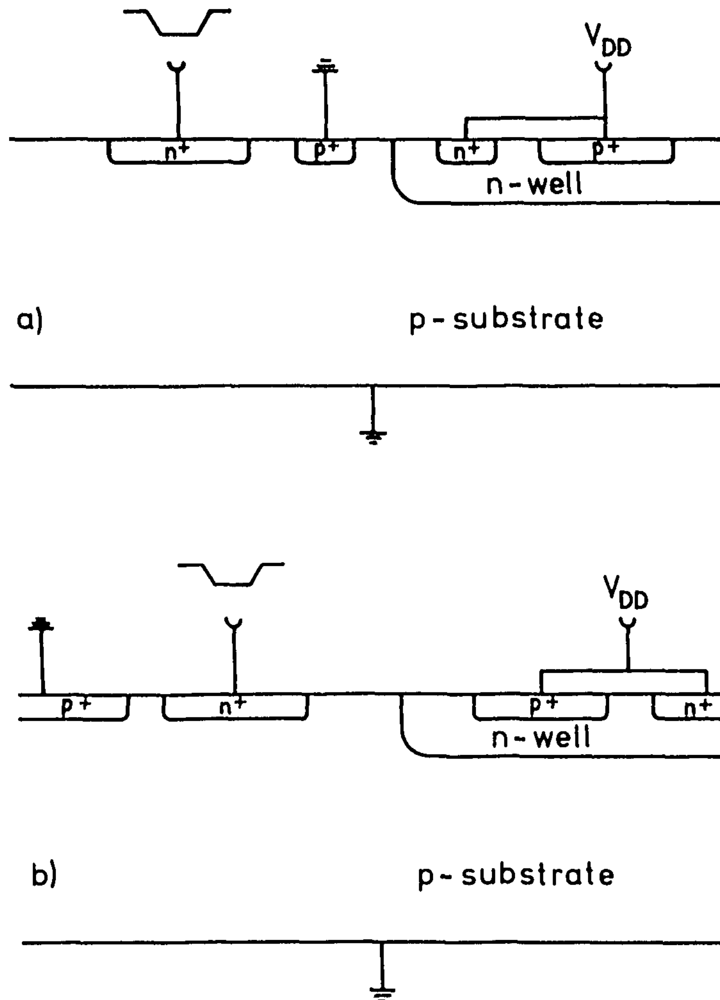


Fig. 1: Schematic cross sections of the test structures a) with guard rings, b) without guard rings.

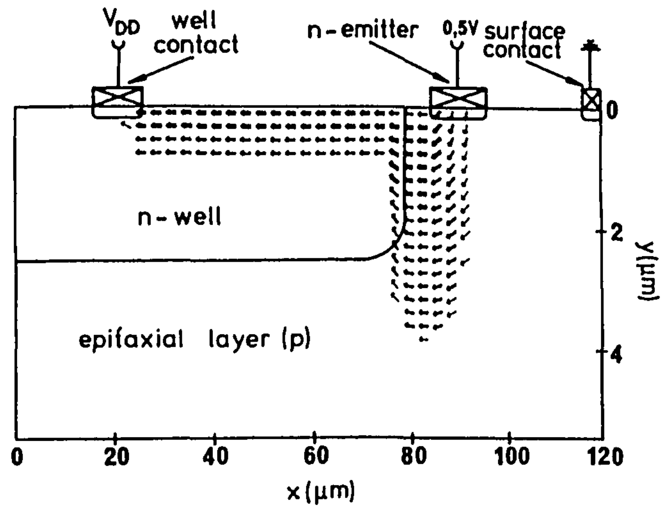
The nonplanarity of the devices was neglected in the BAMBI simulations. The discretization of the structures was accomplished with about 2500 mesh points (finite boxes method) covering a simulation area of 100 x 100 μm^2. Typical CPU times for a transient analysis with 60 time steps were approximately 10 h on a 4.4 MOps computer.

3. NUMERICAL SIMULATIONS

3.1 Structures with epitaxial layer

a) DC characteristics

By placing an epitaxial layer on top of a highly doped substrate, the substrate shunt resistance is strongly reduced, thus acting as an efficient sink for the collector current of the vertical parasitic bipolar transistor.
The substrate is also the base region of the lateral bipolar transistor. We find experimentally that the current gain β of this transistor is higher for devices with an epitaxial layer compared to identical structures on a 10Ω cm substrate. This seems to be in contradiction to simple bipolar models because an eventual outdiffusion of the highly doped region into the epitaxial layer should result in a lower β due to the higher Gummel number in the base region.
However, the reason for the increase in β can be derived from the simulation results in Figs. 2 and 3. In these simulations the lateral transistor was operated at U_{BE} = 0.5V (n-emitter to substrate) and U_{CE} = 5V (n-well to substrate). The surface and backside substrate contacts were grounded. The 2-D electron current density distribution and equipotential contour lines are shown for a structure with (Fig. 2) and without an epitaxial layer (Fig. 3).
In the structure with an epitaxial layer (Fig.2) the electron current path is confined to a region 5 μm in depth, corresponding to the thickness of the low doped region. In the lateral direction, the width of the current path is about 10 μm. The electron current is always directed towards the n-well.
At the boundary between the epitaxial layer and the highly doped substrate the equipotential contours (Fig. 2b) show the built-in potential well due to the gradient in doping concentration. This potential well helps in confining the electrons to the surface region.
In contrast, in the structure without epitaxial layer (Fig.3) electrons are injected down to about 50 μm (not fully shown in Fig. 3a) due to the higher diffusion length in the low doped substrate. The current path extends to about 50 μm in lateral direction. A considerable amount of electrons flows into the direction of the p-surface contact and does not reach the n-well.



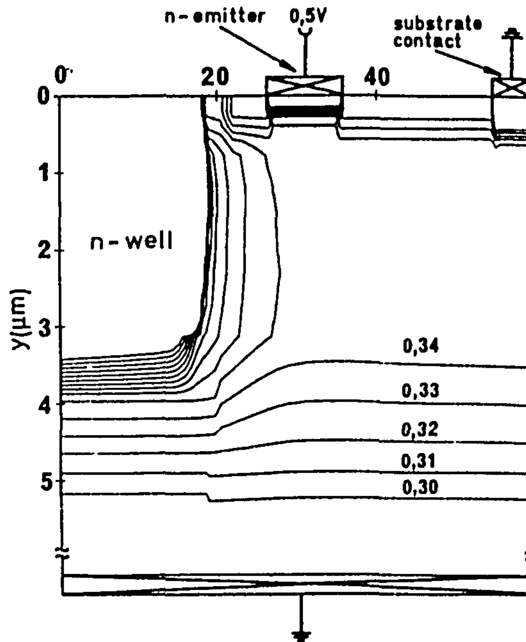
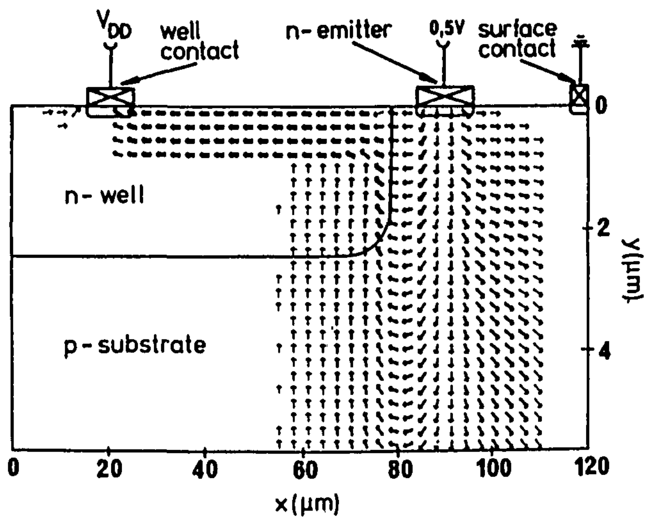


Fig. 2: DC simulation of the lateral bipolar transistor for the structure with an epitaxial layer at U_{BE} = 0.5V, U_{CE} = 5V
a) electron current density distribution
b) equipotential contour lines.



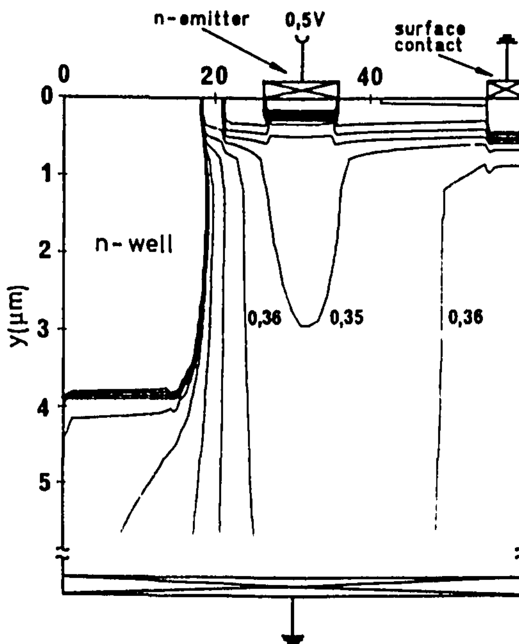


Fig. 3: DC simulation of the lateral bipolar transistor for the structure without epitaxial layer at $U_{BE} = 0.5V$, $U_{CE} = 5V$
a) electron current density distribution
b) equipotential contour lines

It is clear from these observations that the recombination volume for the electrons is much larger in the structure without an epitaxial layer.
Moreover, the base (hole) current from the p-surface contact to the n-emitter region induces a lateral voltage drop (Fig. 3b) which adds a drift component to the electron current in the direction of the p contact. The importance of the drift term ("field-aided effect") has already been stressed by several authors for the latch-up state, where the field component points to the opposite direction /3, 6/.
In the structure with an epitaxial layer the lateral voltage drop is shorted out by the low substrate resistance. The base current is supplied exclusively via the backside substrate contact.
The simulations have shown that all these geometrical and electrical second order effects tend to decrease the base current in the structure with an epitaxial layer, leading to an increase in current gain.
Although the increase in current gain leads to a higher α-product for the parasitic thyristor, the increase in latch-up suceptibility is compensated by the low substrate resistance.

b) Dynamic behaviour

To study the dynamic behaviour of the test structure with an epitaxial layer, an undershoot pulse of -2V magnitude and 8 ns duration was applied to the n-emitter in the substrate (cf. Fig. 1b). The p-emitter and the n-well contact were kept at 5 V whereas the surface and backside substrate contacts were grounded. Fig. 4a) shows the time dependence of the contact currents during the firing phase of the parasitic SCR, simulated with BAMBI. For comparison, the results for a structure without epitaxial layer (same device geometry) are shown in Fig. 4b) for a -4V pulse of 8 ns duration.
For the structure without epitaxial layer (Fig. 4b) the currents from the injecting n-emitter and from the p surface substrate contact are approxiamtely equal and of opposite sign which indicates the build-up of charge in the diffusion capacitance of the lateral bipolar transistor. Current flow from the vertical bipolar transistor (p-emitter) starts at about 5 ns. At this time the electron current reaching the n-well is sufficiently high to achieve a forward bias for the vertical bipolar transistor: the feedback loop for latch-up is closed. A sustaining mode is reached at about 20 ns (not shown in Fig. 4b).
In the structure with an epitaxial layer (Fig. 4a), the hole current for the charging of the diffusion capacitance is supplied exclusiv ely via the backside substrate contact. The same observation was also made for the base current in the dc simulations described above.

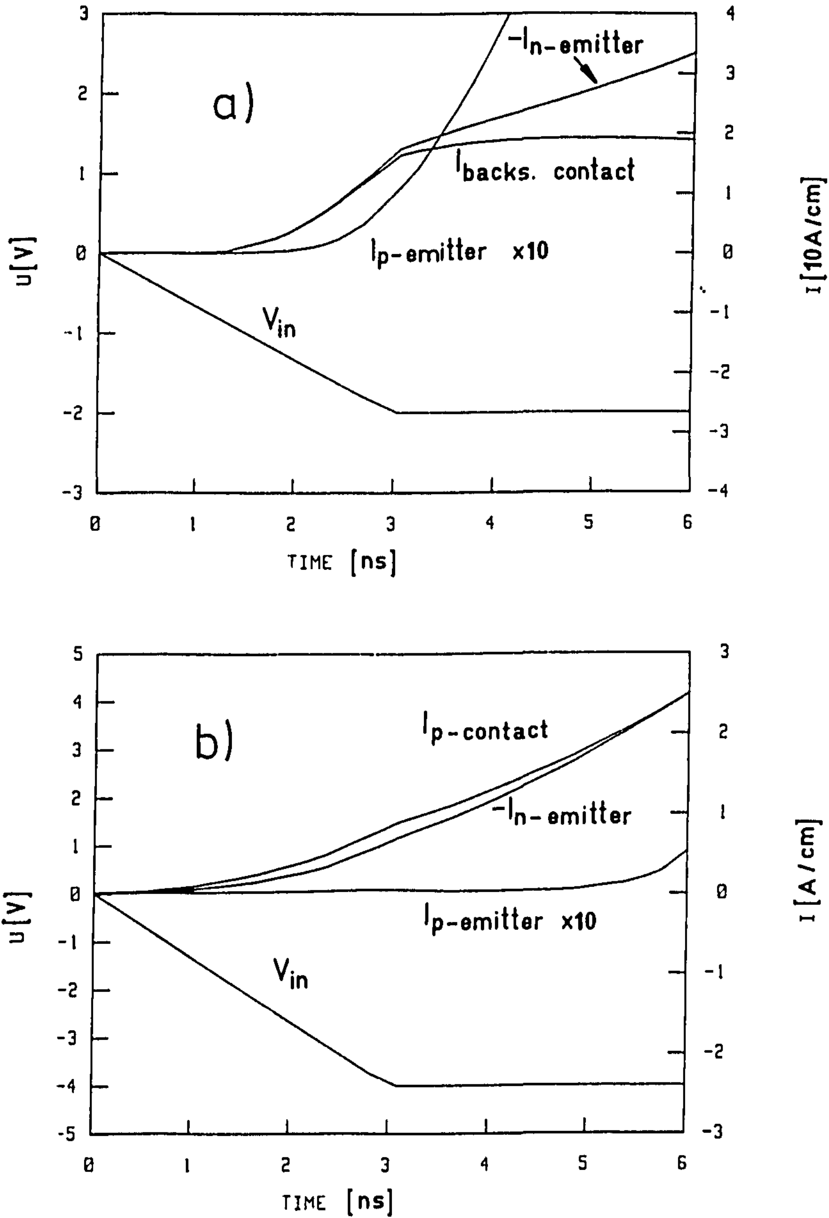
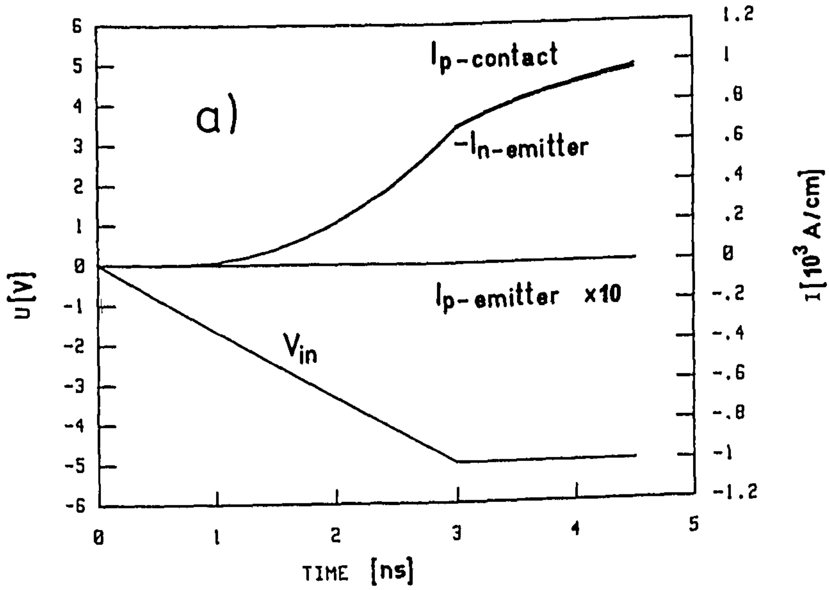


Fig. 4: Contact currents and triggering pulse as a function of time (BAMBI simulations)
a) with an epitaxial layer,
b) without epitaxial layer.

The injection of holes from the p-emitter now already starts at 3 ns. Obviously, the electron current level in the n-well which is needed to achieve a sufficient forward bias for the vertical transistor is reached in a shorter time than in the structure without an epitaxial layer.
From these observations it appears that the charge build-up in the base region of the lateral transistor and, consequently, the beginning of collector current flow is considerably faster in structures with an epitaxial layer. This is due to the low substrate shunt resistance (reducing the relevant time constants) and to the increase in current gain.
For the triggering conditions used in the simulation the use of an epitaxial layer thus results in a faster charge loss from storage nodes due to the thyristor current. The difference in charge loss compared to structures with low doped substrates increases with decreasing pulse width and decreasing epitaxial layer thickness.
In real circuits, however, the difference in charge loss may vanish if the triggering pulse is limited to a low current level, e.g. by series resistances.

3.2 Structures with guard rings

The dynamic latch-up behaviour was studied for a structure with well and substrate contacts arranged adjacent to the well/substrate junction. The simulation results are compared to a similar structure with the conventional arrangement of the contacts. (Note that these structures differ in the n^+/p^+ emitter spacing).
An undershoot pulse at the n emitter in the substrate (magnitude -5V, duration 8 ns) was chosen as a triggering pulse for both structures. The p-emitter and the well contacts were kept at 5V with the surface and backside substrate contacts grounded.
The contact currents as a function of time, simulated with BAMBI, are shown in Fig. 5a) for the structure with guard rings and in Fig. 5b for the conventional structure.
In both structures the currents from the injecting n-emitter and the p surface contacts are equal and of opposite sign. This is characteristic for the charge build-up in the lateral bipolar transistor (cf. section 3.1). In the structure with conventional contact arrangement (Fig. 5b), current flow from the vertical bipolar transistor starts at about 4 ns, indicating the beginning of positive feedback.
In contrast, no current from the vertical transistor is observed for the structure with guard rings (Fig. 5a) up to 5 ns. The reason for this difference is seen in Fig. 6 where the 2-D electron current density distribution is plotted for both structures at t = 1.9 ns.
The structure without guard rings shows a lateral current flow below the p-emitter in the n-well to the well contact



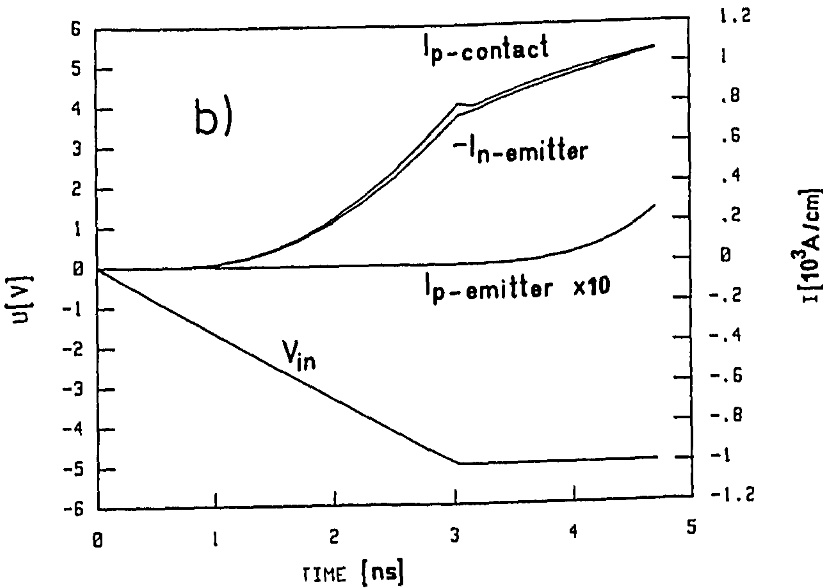


Fig. 5: Contact currents and triggering pulse as a function of time (BAMBI simulations)
a) with guard rings, b) without guard rings.

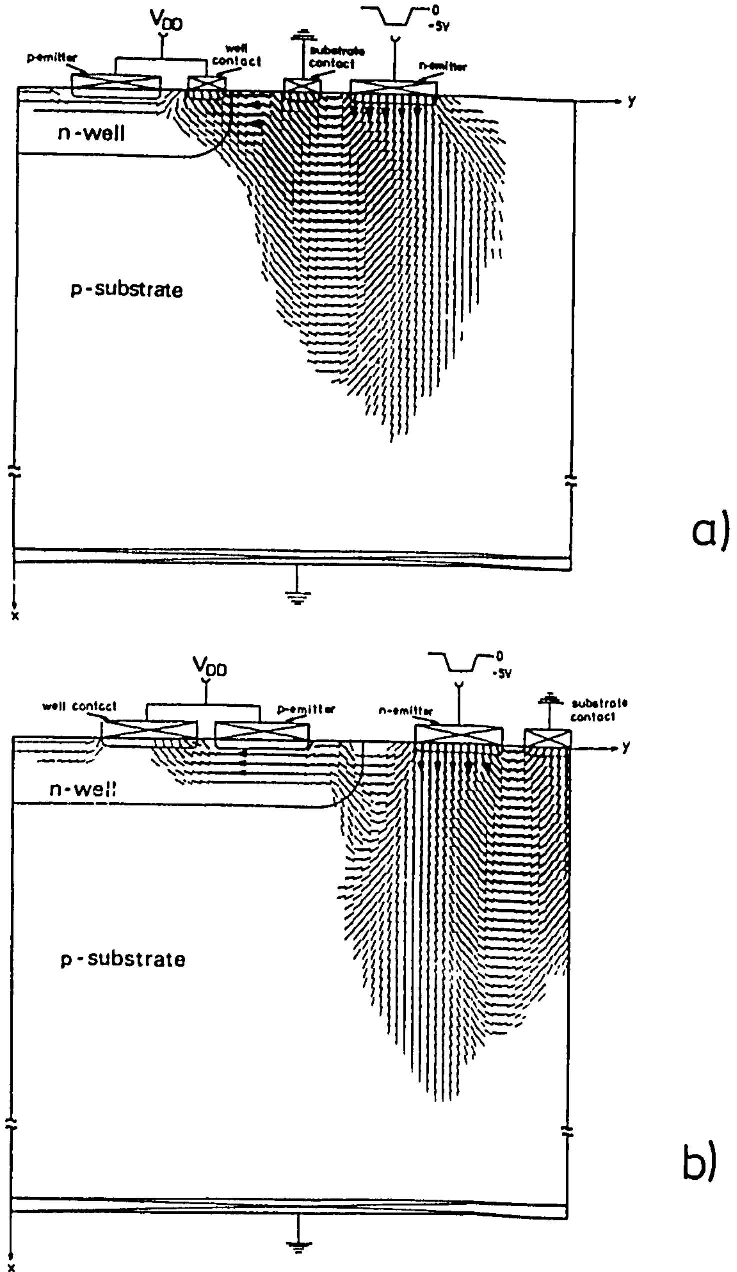


Fig. 6: Electron current density distribution at t = 1.9 ns
a) with guard rings, b) without guard rings.

(Fig. 6b). The voltage drop due to this current establishes a forward bias for the vertical bipolar transistor in the well.
In the structure with guard rings the electron current from the lateral bipolar transistor reaching the n-well is collected efficiently by the n-guardring at the well edge (Fig. 6a).
The small lateral current below the p-emitter is a displacement current which is too small to achieve a sufficient forward bias. The feedback loop of the latch-up path remains open.
At sufficiently high pulse amplitudes and/or durations the current path of the lateral bipolar transistor extends deeper into the bulk as sketched in Fig. 7. Eventually, lateral current flow will start below the p-emitter which may result in a sufficiently high forward bias. For these conditions, a stationary latched state may be reached.
The influence of the p-guard contact in the substrate was not studied separately. The reduction of the substrate shunt resistance should lead to a faster build-up of charge in the lateral bipolar transistor, similar to the effects observed for the structure with an epitaxial layer (cf. section 3.1).

4. CONCLUSION

The dynamics of latch-up firing in VLSI CMOS structures with design variations for latch-up suppression has been studied by 2-D transient device simulations.
The work has shown that many experimental results which could not be understood by simple analytical or 1-D latch-up models, were well reproduced by the 2-D transient simulations and have led to an improved understanding of second order effects on latch-up triggering.

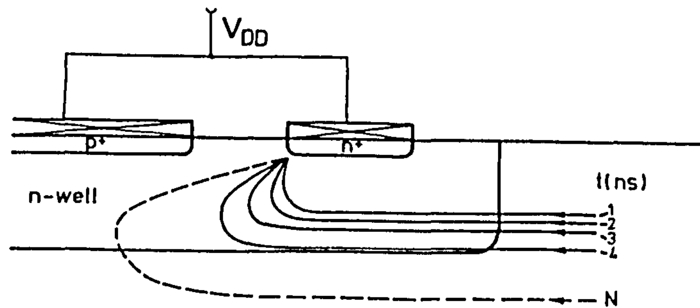


Fig. 7: Extension of the lateral electron current path at the n-well boundary as a function of time for the structure with guard rings.

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