LATERAL POWER MOSFET WITH AN IMPROVED ON-RESISTANCE

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ABSTRACT

The product of the on-resistance by the area of the high-voltage, LDMOS transistor can be reduced by a factor of two to four by creating a surface accumulation layer along the surface of the drift region. This surface accumulation region exists only in the on state of the device. It can be created by using a semi-insulating layer over a thin field oxide layer covering the drift region, or alternatively via a fourth electrode located between the drain and the gate, and held at a constant high voltage. Henceforth, a simple LDMOST structure with no critical processing steps, low on-resistance and high breakdown voltage is claimed.

1. INTRODUCTION

Power MOSFET's have several advantages over their bipolar counterparts including thermal stability, high power gain, high speed response, and the ease of paralleling MOSFET's. However, for the same breakdown voltage and the same chip area (i.e., price), the power MOSFET can only deliver an on-state current which is one-fifth that of the bipolar power transistors [1]. To overcome this major drawback of the power MOSFET's, the conductivity modulated FET (COMFET) [1-2] was developed in which a p-n junction is "hooked" to drain side of the power MOSFET. In the on-state of the device, this "hooked" junction acts as a high-level injector of minority carriers into the drift

region of the transistor, and thus modulates its resistance. In this paper, we present an alternative solution to the high on-resistance (R_{on}) of lateral power MOSFET. This alternative solution [3] is based on modulating the resistance of the drift region by majority carriers rather than by minority carriers as is described in [1-2].

2. PRINCIPLE OF OPERATION:

Our proposed technique for reducing $R_{on}A$ for a lateral power MOSFET is based on creating a heavy accumalation layer over the whole of the drift region of the LDMOST. This accumulation region exists only in the on-state of the device.

The prior art of the LDMOST design (without any conductivity modulation feature) is described in Ref. [4,5]. Fig.[1] depicts such design which suffers from a well known trade-off between the R_{on} * Area ($R_{on}A$) and the breakdown voltage of the device. In particular the spacing,d, between the gate overlay and the drain overlay [Fig.(1)] should be large enough to avoid premature breakdown. At the same time, d, should be kept as small as possible to achieve low $R_{on}A$.

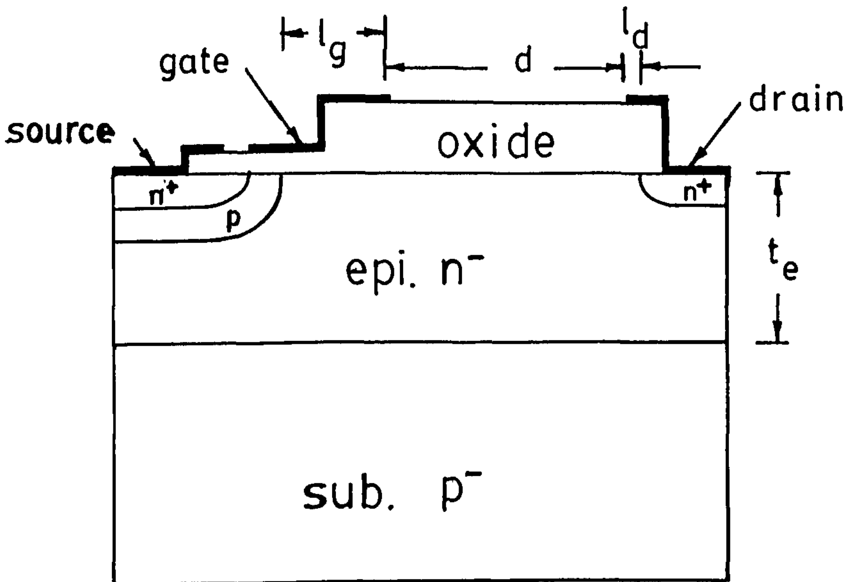


Fig. 1 The classical RESURFed LDMOST. l_g is the gate overlay, l_d is the drain overlay and t_e is the epi-layer thickness

Our proposed design is depicted in Fig.(2a). A semi-insulating layer of polysilicon (SIPOS) is deposited over the oxide layer covering the surface of the drift region. In the off-state, the potential drop between the drain and gate is uniformly distributed along the SIPOS layer [Fig. (2b)]. Consequently the surface electric fields in the semiconductor are reduced [6]. However, the beneficial effects of this SIPOS layer are much more important in the on-state. The potential distribution in the latter state is shown in Fig. (2c). The SIPOS layer acts now as a "extended" gate finger reaching to the drain causing an accumulation region to build up at the surface of the drift region. This accumulation layer acts to reduce the on-resistance of the device. It may be noted that the sheet resistance of this surface accumulation layer is directly proportional to the thickness of the oxide under the SIPOS layer. Therefore, this oxide thickness has to be reduced from ~ 1 μm typically used in the ordinary LDMOST design to ~ 1000 ^{o}A or less in this design. It may be noted that the breakdown voltage of the LDMOST is adversely affected by this reduction of the oxide thickness. Rigorous comaprison [7] of the proposed LDMOST and the classical LDMOST is further discussed in section 4.

This new power LDMOST structure is named the Accumulation LDMOST or briefly ALDMOST.

3. DEVICE MODELLING

3.1. On-resistance

A simple one dimentional model for the on-resistance, R_{on}, of the ALDMOST is now described. R_{on} is considered to be that of the drift region and is composed of two parallel resistances, the bulk resistance and the accumulation layer resistance. The bulk resistance, R_b, may be calaulated by conformal mapping [4] or more accurately by a 2-D finite element analysis of the current flow in the drift region [8]. The accumulation resistance, R_a, present only in the ALDMOS structure, may be found by integrating this layer resistance along the length, L_a, of the drift region covered by the SIPOS layer. The following expression for R_a can thus be derived.

$$R_a = \frac{L_a}{ZK} \frac{1}{(V_G + |V_{fb}|)} \ln\left(1 + \frac{V_G}{|V_{fb}|}\right) \qquad (1)$$

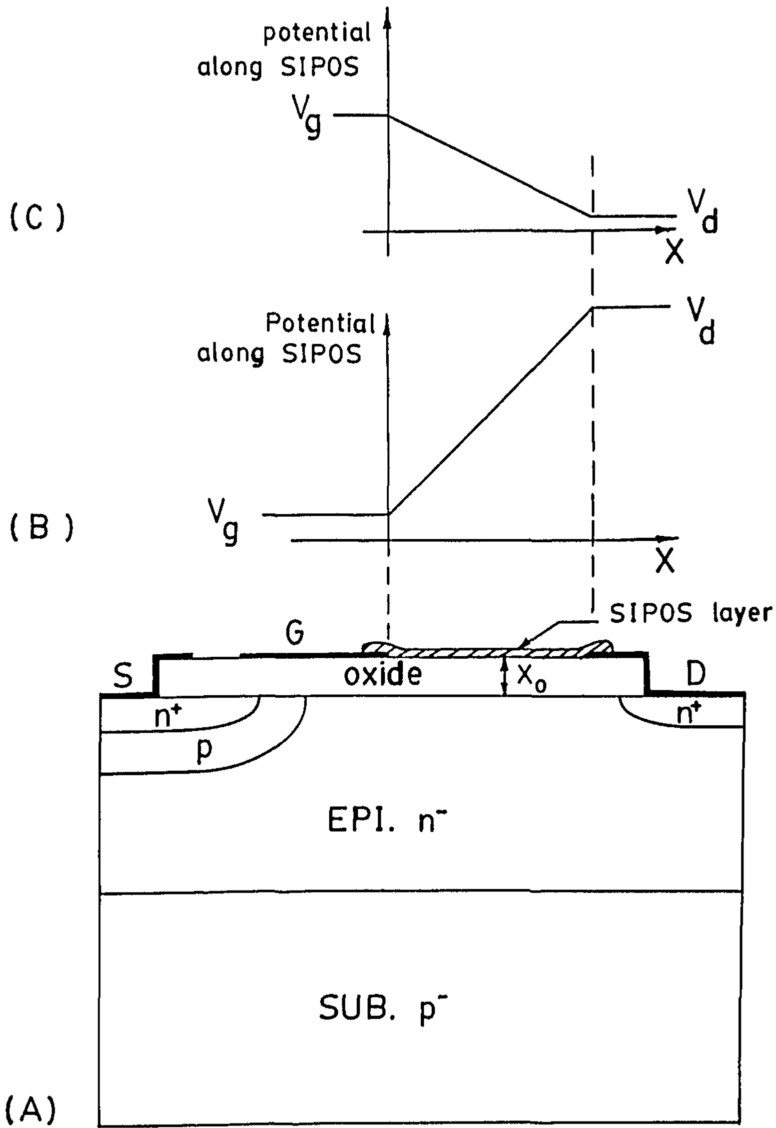


Fig. 2.(a) The proposed structure of the ALDMOST. x_0 is~ 500 → 1000°A.
(b) The voltage distribution across the SIPOS layer in the off-state.
(c) The voltage distribution across the SIPOS layer in the on-state.

where Z = width of the drift region

$$k = \frac{\mu_n^* \epsilon_i}{x_o}$$

where μ_n^* = surface mobility of the majority carriers.

ϵ_i = permitivity of the insulating region.

x_o = the thickness of the insulating region.

V_{fb} = the flat-band voltage of the SIPOS-insulator-n Si. V_{fb} is assumed negative.

V_G = gate voltage.

Further more , R_b satisfies the inequality

$$R_b > L_a / \sigma_b Zd \qquad (2)$$

where σ_b is the bulk conductivity of the drift region. The ratio of the on-resistance with an accumulation layer ($R_a // R_b$) to that without an accumulation layer, R_b, may be taken as a measure, M, of the effectiveness of the accumulation layer for the reduction of R .

$$M > \frac{R_a}{(R_a // R_b)} = 1 + \frac{R_a}{R_b} \qquad (3)$$

Note that a small thickness of the insulator region, and a high value of ϵ_i are needed to enhance M.

Accurate 2-D FEM simulation for the current flow in the drift region of both the ALDMOST and the ordinary LDMOST has also been carried out [7]. Hybrid FEM formulation was utilized with linear 3-noded elements for the surface accumulation layers and 2-D, 8-noded isoparametric elements for the bulk of the drift region. Thus, R_{on} was accurately calculated with and without the surface accumulation layer. Fig.(3) depicts the varation of R_{on} with the gate voltage for the ALDMOST and the classical LDMOST of Colak [4,5]. The geometry and dopings of the classical LDMOST (cf. Fig.(1)) are given in the caption of Fig.(3). The ALDMOST has an identical structure except for the oxide thickness over the drift region which is reduced to 500 ^{o}A . The beneficial reduction in R_{on} by the simple ALDMOST technique is obvious.

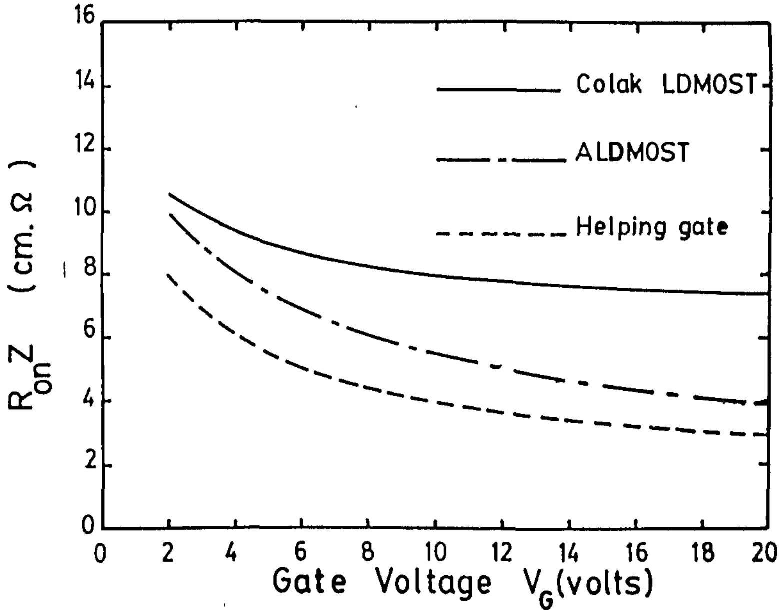


Fig. 3. Calculated $R_{on}Z$ for the ALDMOST and the classical LDMOST of Colak [Fig.(1)]. The substrate doping N_a = the epi-layer doping, $N_d = 1.2 \times 10^{15}$ cm^{-3}, epi-layer thickness = 15μm, d = 12μm, l_g = 14μm, and the unit cell length = 50μm

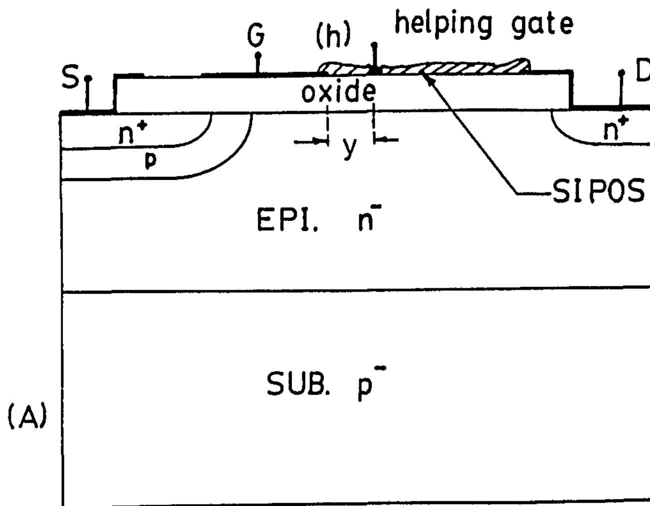
3.2. Breakdown Voltage

It has already been stated that the figure of merit, $R_{on}A$, of the power LDMOST has to be calculated at a constant breakdown voltage rather than for a constant geometrical and doping details as in Fig.(3). We have used the SWANOFF2 [9] package to calculate breakdown voltage of the ALDMOST and classical LDMOST accurately.

4. Evolved ALDMOST structures

The princple of the reduction of the on-resistance via a surface accumulation layer can be further enhanced as follows : Let the potential at a given position y in the SIPOS layer be V when the MOSFET is off. The potential distribution, and hence, the breakdown voltage of the LDMOST is not affected by the intrduction of a "helping"

electrode at the same position y and biased with the same voltage. However, if this "helping" electrode is maintained at the high voltage, V, when the ALDMOST is turned on, a significant reduction in the on-resistance takes place [Fig.(3)]. The structure of the ALDMOST with the helping electrode is shown in Fig.(4a). Fig.(4b) depicts the required bias connection for the helping electrode. A polysilicon potential divider R_2 and R_3 may be advantageously built on the chip, which should now be provided with an extra pin for the supply voltage. In choosing the location, and hence, the fixed bias V of the helping electrode, care must be exercised to insure that the voltage V, which is almost totally dropped across the insulator in the on-state, is smaller than the breakdown voltage of the insulator region.



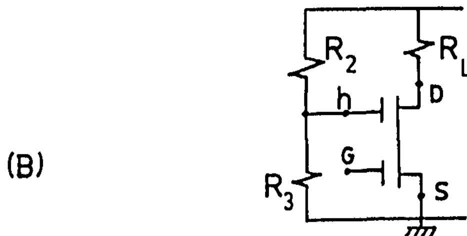


Fig. 4. (a) The ALDMOST structure with a helping gate (or electrode)
(b) The required bias arrangement. R_L is the load.

Consider next the ALDMOST of Fig.(2). Both its RESURF structure and its field shaping SIPOS layer act to reduce the surface electric fields. In fact, the SIPOS layer tends to achieve the ideal case of uniform surface fields between the body region and the drain region. Consequently, the RESURF structure may be dropped leading to the simple ALDMOST structure of Fig.(5). This simple structure achieves a high breakdown voltage due to the field shaping effect of the SIPOS as well as a low on-resistance due to the accumulation layer formation. It also offers the advantage of uncritical fabrication tolerance with respect to the RESURFed structure. This embodiment of the ALDMOST principle was rigoriously compared to the ordinary LDMOST. Two-dimensional FEM calculation of R_{on} for the two devices was carried out keeping their areas and breakdown voltages fixed. Fig.(6) shows the constant voltage contours of ALDMOST at its breakdown voltage of 375 V. Fig.(7) depicts R_{on} variation with the gate voltage for both devices. The advantage of using the ALDMOST approach especially with a helping electrode is clearly evident. The accumulation layer can be further enhanced by using a sandwich of SiO_2/Si_3N_4 instead of SiO_2.Fig.(8) shows $R_{on}A$ for the ALDMOST with a SiO_2/Si_3N_4 sandwich, and clearly demonstrates the enhanced on-state conductance.

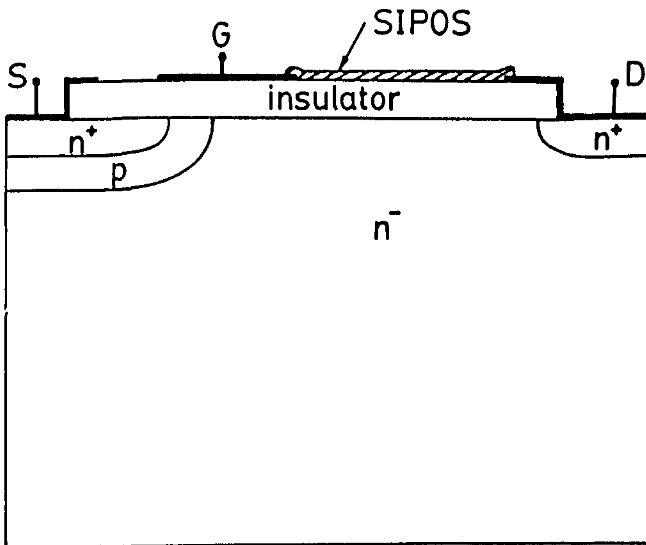


Fig. 5. Simple non RESURFed ALDMOST structure

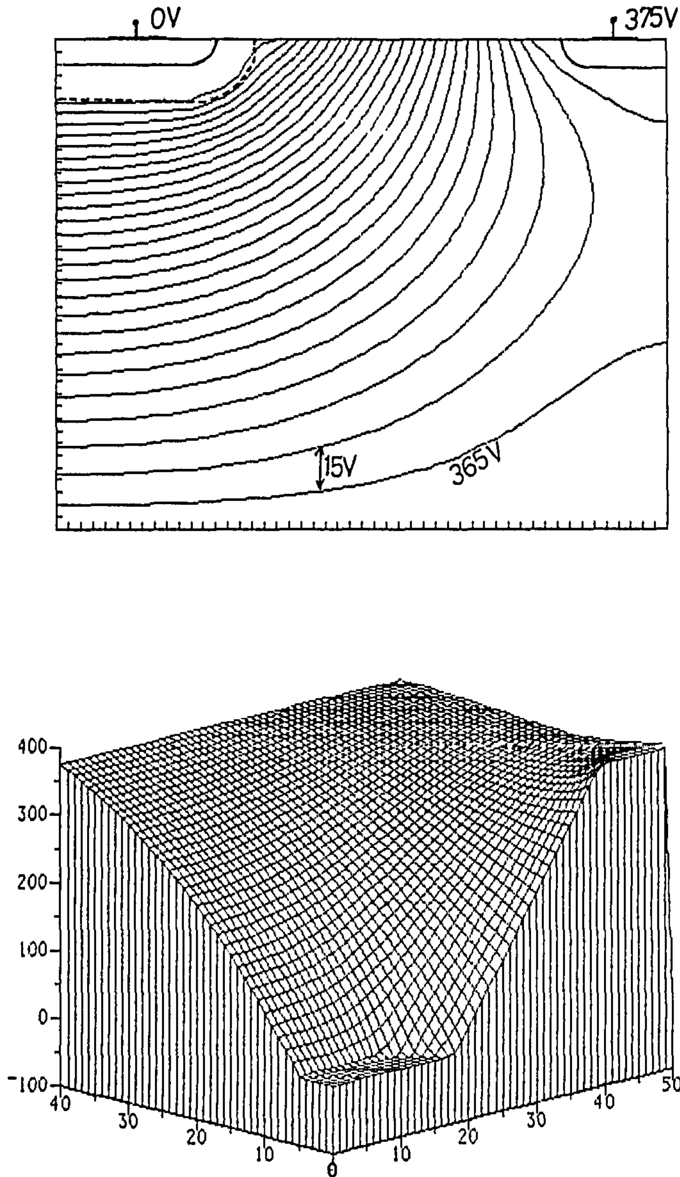


Fig. 6.(a) The equipotential contours of a non RESURFed ALDMOST at its breakdown voltage of 375 V. N $=1.1*10^{14}$ cm^{-3}, the body-drain spacing = 25μm and the the unit cell length = 50μm.

(b) 3-D picture of the potential distribution of (a).

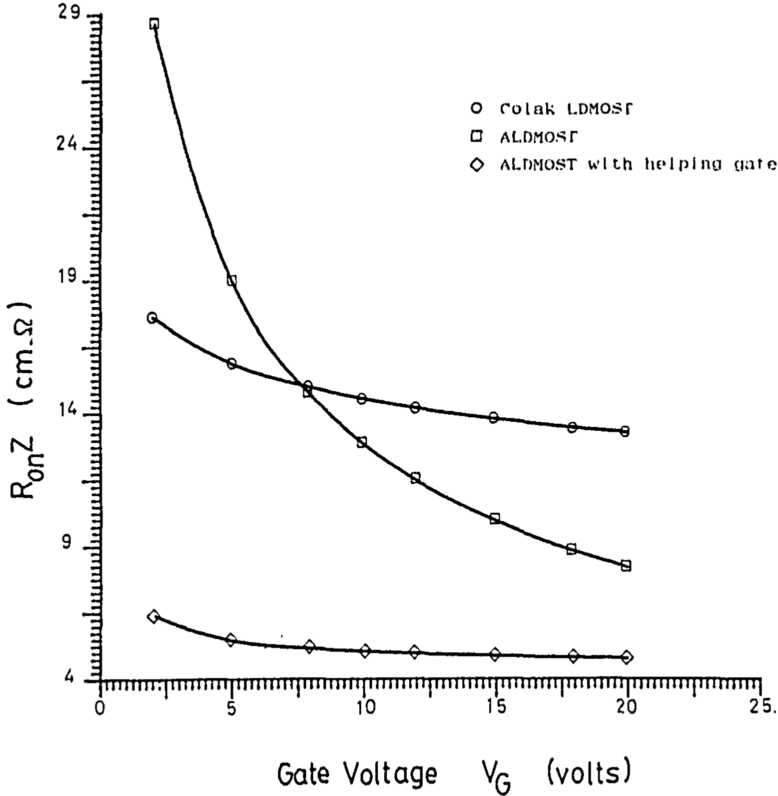


Fig. 7. Calculated R_{on} Z for the ALDMOST of Fig.(5), and an optimized classical LDMOST with the same breakdown voltage (375 V) and the same unit cell length (50 μm). For the classical LDMOST [Fig.(1)], d=17.5μm, l_g =8μm, l_d =1.5μm, N_d =0.95*10^{15} cm , N_a =1.1*10^{15} cm ,the body and drain junction depths are 5 and 2 μm's respectively. The field oxide thickness=1 μm. For the ALDMOST, the insulator is SiO_2 and its thickness is 500 °A. The helping gate is biased at 40V and located at 2 μm away from gate overlay.

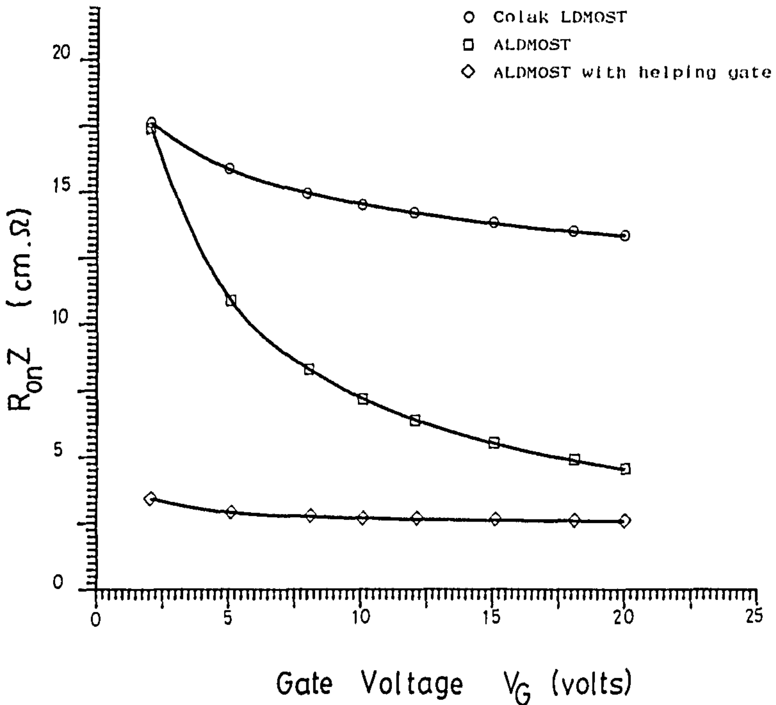


Fig. 8. Calculated $R_{on}Z$ for the ALDMOST and the classical LDMOST. The same device parameters as in Fig.(7) except for the insulator of the ALDMOST which is here a swandwich of 50°A of SiO_2 (ϵ_i=3.9ϵ_0) and 400°A of Si_3N_4 (ϵ_i=7.5ϵ_0)

Conclusions

A new MOS-based method for breaking the traditional trade off between $R_{on}A$ and breakdown voltage of a high voltage LDMOST is proposed. This methods depends on creating a shunting majority carrier layer across the LDMOST surface in the on state only. This new method offers the advantages of low $R_{on}A$ and the ease of Fabrication. Since this method relies on majority carriers, it maintains the excellent temperature stability characteristics of the MOS devices.

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