AN INVESTIGATION ON POLYCRYSTALLINE-SILICON MOSFET OPERATION

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Abstract

In this paper we investigate the physical properties of polycrystalline-silicon MOSFETs by means of a two-dimensional device-analysis program called HFIELDS. Grain-boundaries are treated by the code as semiconductor-semiconductor interfaces where monovalent donor and acceptor states can be accomodated. The trapped charge influences electric potential via Poisson's equation, and contributes to generation currents within the device itself according to SRH statistics. A simplified MOSFET model is developed, by converting the grain boundary traps into an equivalent amount of bulk-distributed generation-recombination centers. The simplified model is shown to agree with numerical results only when the thickness of the film is large enough to justify the assumption of charge neutrality at the back-oxide interface.

1. Introduction

Polycrystalline-silicon thin-film transistors have been widely investigated in the last few years as possible candidates for three-dimensional integration and as active elements in liquid-crystal flat-panel displays [1,2]. However, potential advantages of dielectric isolation, such as higher packing density, increased radiation tolerance, and latch-up immunity are presently offset by major drawbacks, such as low carrier mobility, short carrier lifetimes, high leakage currents and large threshold voltages.

In order to overcome the above problems, much effort has been devoted to improving the quality of the film. Zone melting recrystallization [3,4] has been used to increase the grain size, and hydrogen passivation has resulted in reduced grain-boundary trap densities [1]. Nevertheless, the overall performance achieved thus far cannot be considered fully satisfactory.

In the authors' view, a better understanding of device behaviour is necessary to provide clever device designs. Consequently, we have incorporated in our two-dimensional simulation code a simplified grain-boundary model accounting for monovalent generation-recombination centers, both donors and acceptors [5,6]. The program was then used to simulate two polycrystalline-silicon MOSFETs having film thicknesses of $1.0\,\mu m$ and $0.1\,\mu m$, respectively.

Following a suggestion by Depp *et al.* [7], a simplified model based on an equivalent number of bulk-distributed generation recombination centers has also been developed in this paper. The obtained results, however, confirm that the simplified model can successfully predict the device characteristics only for relatively thick semiconductor

films and in strong inversion conditions.

In the next Section, the physical model of grain-boundary incorporated in the code is illustrated. In Section 3 we derive the MOSFET current-voltage characteristics using the bulk-distributed trap model. Section 4 contains a description of our simulation results for both semiconductor-film thicknesses and comparisons between numerical results and the simplified model. Discussion of the above results and conclusions follow in Section 5.

2. Numerical Model

The grain-boundary model to be incorporated in a general-purpose device-analysis tool should be, as far as possible, consistent with the fundamental device equations solved by the program. For the above reason, we decided to treat grain boundaries as strictly two-dimensional interfaces where a large amount of donor and acceptor states can be accomodated [8-10]. The charge trapped in these states influences the electric potential distribution via Poisson's equation; carrier transport occurs instead according to the drift-diffusion mechanism, as in standard single-crystal devices. A discussion on the adequacy of the present model is contained in [6].

The program solves the following set of partial differential equations

$$\operatorname{div}(\epsilon_s \operatorname{grad}\varphi) = -q\,(p - n + N_D^+ - N_A^-) - Q_{it}\delta(\mathbf{r} - \mathbf{r}_i) \tag{1a}$$

$$\frac{\partial n}{\partial t} - \operatorname{div}(\mathbf{J}_n/q) = (G - R) + (G - R)_i\delta(\mathbf{r} - \mathbf{r}_i) \tag{1b}$$

$$\frac{\partial p}{\partial t} + \operatorname{div}(\mathbf{J}_p/q) = (G - R) + (G - R)_i\delta(\mathbf{r} - \mathbf{r}_i) \tag{1c}$$

comprising Poisson (1a) and carrier-continuity equations for electrons (1b) and holes (1c). In eqns. (1) the symbols are given the usual meaning, namely: φ is the electric potential, n and p are the electron and hole concentrations, respectively, $N_D^+ - N_A^-$ is the net ionized impurity concentration, Q_{it} is the trapped charge density per unit area, $\mathbf{r}_i$ denotes the interface regions, $\mathbf{J}_n$ and $\mathbf{J}_p$ are the electron and hole current densities, $(G - R)$ is the net generation rate per unit volume and $(G - R)_i$ is the net recombination rate per unit area.

Current densities are expressed via the usual drift–diffusion equations, viz.

$$\mathbf{J}_n = -q\mu_n n \operatorname{grad}(\varphi + \Delta\varphi_c) + qD_n \operatorname{grad} n \tag{2a}$$

$$\mathbf{J}_p = -q\mu_p p \operatorname{grad}(\varphi - \Delta\varphi_v) - qD_p \operatorname{grad} p, \tag{2b}$$

where μ_n and μ_p represent the electron and hole mobilities; D_n and D_p are the electron and hole diffusivities, related to mobilities by the Einstein relations and $\Delta\varphi_c$, $\Delta\varphi_v$ represent the shift in the conduction/valence band edges due to heavy doping. If bandgap narrowing is neglected, $\Delta\varphi_c = \Delta\varphi_v = 0$, and the force acting on carriers is simply due to the electric field. In eqns (1), the trapped charge Q_{it} is given by

$$Q_{it} = -qN_{it}\,\frac{s_n n + s_p p_1}{s_n(n + n_1) + s_p(p + p_1)} \tag{3a}$$

if the states are acceptor-type, and by

$$Q_{it} = qN_{it}\,\frac{s_n n_1 + s_p p}{s_n(n + n_1) + s_p(p + p_1)} \tag{3b}$$

for donor interface states, and the net generation rate per unit area $(G - R)_i$ is given by

$$(G - R)_i = \frac{n_{ie}^2 - np}{(n + n_1)/s_p + (p + p_1)/s_n} \tag{3c}$$

where the surface recombination velocities s_n, s_p are expressed as $s_n = \sigma_n v_{th} N_{it}$, $s_p = \sigma_p v_{th} N_{it}$, N_{it} represents the interface-state density, σ_n and σ_p are the capture cross sections, v_{th} is the carrier thermal velocity, and n_1, p_1 are defined as $n_1 = n_{ie} \exp[(E_t - E_i)/kT]$, $p_1 = n_{ie} \exp[(E_i - E_t)/kT]$, E_i being the intrinsic Fermi level and E_t the trap energy.

3. Distributed-trap model

A simplified approach to polycrystalline-silicon MOSFET modelling was suggested in [7], where grain-boundary traps are converted into an equivalent number of bulk traps. The analysis developed in [7], however, suffers two major limitations: first, the equilibrium distribution of trapped charge is used for $V_{DS} \neq 0$ and, next, the bulk impurity concentration is ignored compared with the trapped charge.

In this section we review the thin-film transistor model based on distributed bulk traps. The analysis is carried out under the following simplifying assumptions:

- The gradual channel approximation is assumed to hold;
- The electron quasi-Fermi potential is spatially constant normal to the $Si - SiO_2$ interface;
- Homogeneous Neumann boundary conditions are assumed at the bottom-insulator interface;
- The energy of the traps is located at midgap;
- An equivalent concentration of donor and acceptor states is assumed;
- Electron and hole capture probabilities are assumed to be identical.

From the three latter assumptions, the trapped charge density ρ_t can be expressed as

$$\rho_t = -qN_t \frac{c_n(n - n_1) - c_p(p - p_1)}{c_n(n + n_1) + c_p(p + p_1)} = -qN_t \frac{\exp[q(\varphi - \varphi_n)/kT] - \exp[-q\varphi/kT]}{\exp[q(\varphi - \varphi_n)/kT] + \exp[-q\varphi/kT] + 2} \tag{4}$$

where c_n and c_p represent the electron and hole capture probabilities, respectively. The one-dimensional Poisson equation then becomes

$$\frac{d^2u}{dx^2} = \frac{1}{L_i^2}\left\{\exp(u - u_n) - \exp(-u) + \frac{N_A}{n_i} + \frac{N_t}{n_i}\frac{\exp(u - u_n) - \exp(-u)}{\exp(u - u_n) + \exp(-u) + 2}\right\} \tag{5}$$

where $u = q\varphi/kT$ is the normalized potential, $u_n = q\varphi_n/kT$ is the normalized quasi-Fermi potential and $L_i = (\epsilon_s kT/q^2 n_i)^{1/2}$ is the intrinsic Debye length.

A first-integral of eqn (5) can be obtained in closed form

$$\frac{du}{dx} = -\frac{\sqrt{2}}{L_i}\left\{\exp(u - u_n) - \exp(u_h - u_n) + \exp(-u) - \exp(-u_h) + \frac{N_A}{n_i}(u - u_h) + \frac{N_t}{n_i}\log\frac{\exp(u - u_n) - \exp(-u) + 2}{\exp(u_h - u_n) + \exp(-u_h) + 2}\right\}^{1/2} \tag{6}$$

where u_h represents the normalized potential at the bottom-insulator interface. If we assume charge neutrality to hold, u_h is determined by equating to zero the RHS of eqn. (5). This is perhaps the most suspect assumption of the present analysis. We expect such an assumption to hold in the limit of thick polycrystalline-silicon films, where the gate-induced field vanishes at a sufficient depth from the $Si - SiO_2$ interface.

The MOSFET current can finally be expressed by the Pao-Sah [11] double-integral formula

$$I_{DS} = (W/L)kT\mu_n n_i \int_{U_S}^{U_D}\left\{\int_{u_h}^{u_s} \exp(u - u_n)(du/dx)^{-1}du\right\}du_n \tag{7}$$

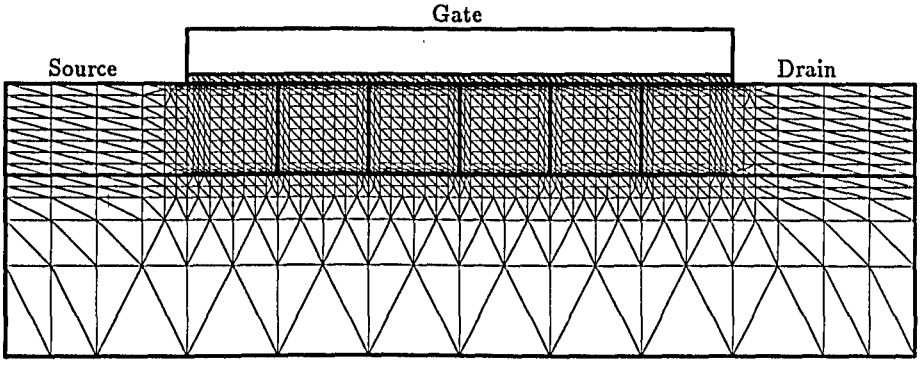

Fig. 1. *Geometrical structure of the simulated polycrystalline-silicon MOSFET. The semiconductor film comprises six crystallites in the channel region. The associated mesh contains 1268 nodes and 2416 elements.*

where U_S and U_D are the normalized source and drain voltages, and u_s represents the normalized surface potential. For each value of u_n, the corresponding surface potential results from the iterative solution of the equation

$$V_G + \varphi_{FG} = (kT/q)u_s - (\epsilon_s kT/qC_{ox})(du/dx)_{u=u_s} \tag{8}$$

φ_{FG} being the Fermi potential in the degenerately-doped poly-gate, and C_{ox} the oxide capacitance.

4. Numerical Results

The $1\,\mu m$ thick polycrystalline silicon MOSFET and the resulting triangular-element grid are illustrated in figure 1.

The thicknesses of the gate oxide and of the bottom insulator are $0.1\,\mu m$ and $2.0\,\mu m$, respectively. Channel length was chosen to be $6.0\,\mu m$ to eliminate short-channel effects, and six cubic crystallites have been considered in the channel region. The grid comprises 1268 nodes and 2416 highly non-homogeneous elements, and is heavily refined at the grain boundaries and at the $Si - SiO_2$ interfaces. One electron and one hole trapping state were assumed at midgap, with a density $N_{it} = 2\times10^{12} cm^{-2}$ at the grain boundaries, and $N_{it} = 4 \times 10^{11} cm^{-2}$ at the $Si - SiO_2$ interfaces. Finally, the bulk impurity concentration was $N_A = 10^{15} cm^{-3}$. Figure 2 shows the electric potential in the channel region in equilibrium conditions, i.e. by assuming $V_{GS} = V_{DS} = 0$. Having assumed a degenerately-doped n^+ polycrystalline-silicon gate, and a Fermi level at the bottom of the conduction band, the gate potential turns out to be $\simeq E_G/2q$, i.e. $0.56\,V$, and the same holds true for the backgate potential. The source and drain potentials, instead, are slightly above $0.56\,V$, as the assumed impurity concentration in these regions is $2 \times 10^{20}\, cm^{-3}$, which exceeds the effective density of states in conduction band. The large trap density pins the trap energy at the Fermi

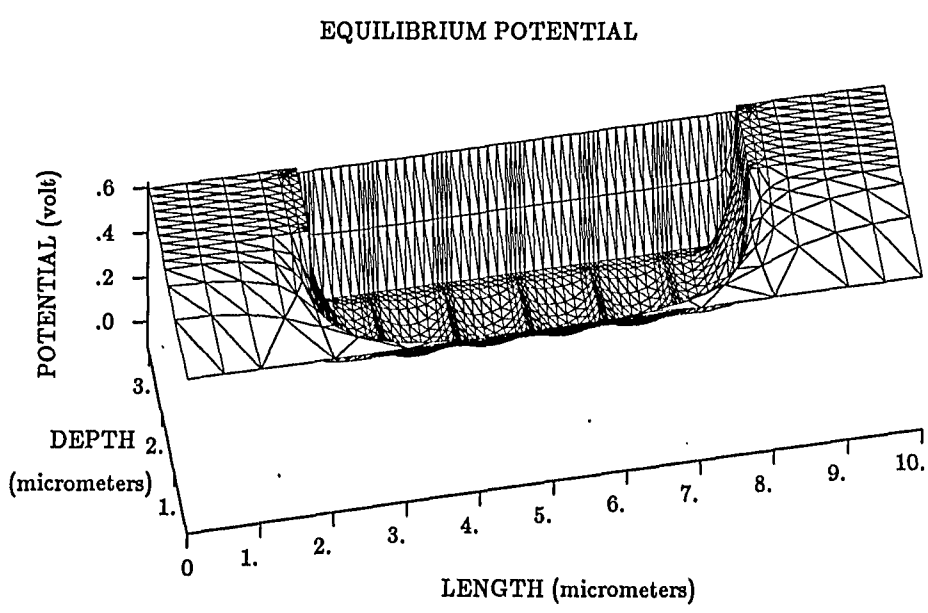

Fig. 2. *Equilibrium electric potential in the simulated structure. The bulk impurity concentration is* $N_A = 10^{15} cm^{-3}$.

level, so that grain-boundary and silicon-silicon dioxide interfaces are very close to zero potential. Due to the small impurity concentration in the channel region, the grains are fully depleted and the minima are well above the equilibrium potential in a neutral region, which equals $-0.289\,V$ for $N_A = 10^{15}\,cm^{-3}$.

Figure 3 shows the electric potential in non-equilibrium conditions below threshold: here $V_{DS} = 0.25\,V$ and $V_{GS} = 2.0\,V$. It is interesting to notice that, in this case, the curvature of the potential inside the grains near the interface is reversed. This effect is due to the simultaneous assumption of both donor and acceptor states both at the $Si - SiO_2$ interface and at the grain boundaries: the field effect due to the gate potential tends to create an inversion layer at the interface. As a consequence, more electron traps are filled, leading to a depletion region near the interface. The electron concentration is shown in figure 4 for the same biasing conditions: it can be clearly seen that, at the grain boundaries, the electron concentration drops down to about n_i, thus preventing a conductive channel to be formed.

Figure 5 shows the electric potential within the structure with $V_{GS} = 6\,V$ and $V_{DS} = 5\,V$, i.e. in strong inversion conditions. Here again we see that the curvature of the electric potential is reversed at the $Si - SiO_2$ interface; besides the potential barriers experienced by channel electrons are now very small, and cannot prevent conduction. Figure 6 shows the electron concentration in the same biasing conditions, and it confirms the existence of a highly-conductive channel at the interface. The effect of drain potential is limited to the last crystallite of the channel, leading to some decrease in electron concentration.

The turn-on characteristics are represented in figure 7 for two values of the drain voltage, namely $V_{DS} = 0.25$ V and $V_{DS} = 5.0$ V. The slope of the curves in the subthreshold region is characterized by an ideality factor n = 2.0 , and the leakage current is in the 0.1 nA range. The effect of carrier generation slightly influences the leakage current, which is mainly due to the pinning of the trap energy at the

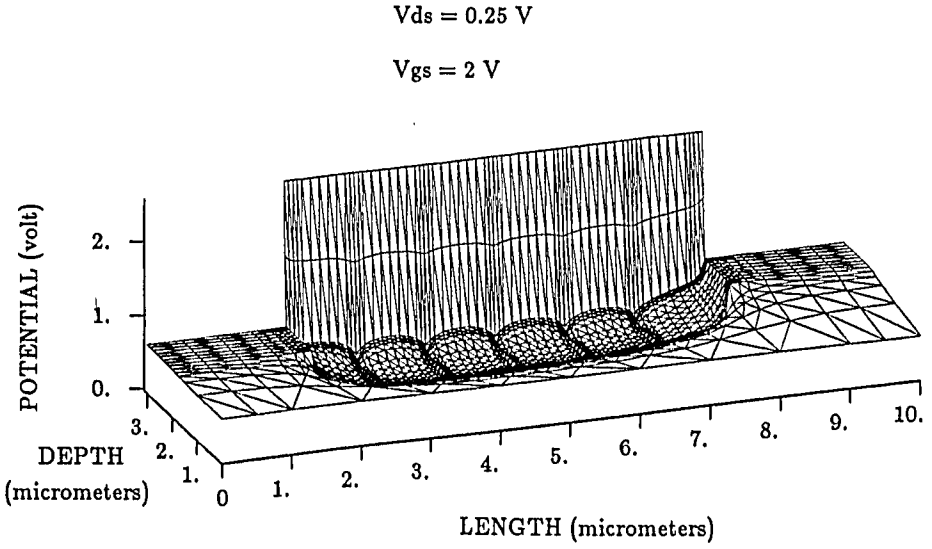

Fig. 3. *Electric potential within the simulated polycrystalline-silicon MOSFET:* V_{GS} = *2.0 V,* V_{DS} =*0.25 V.*

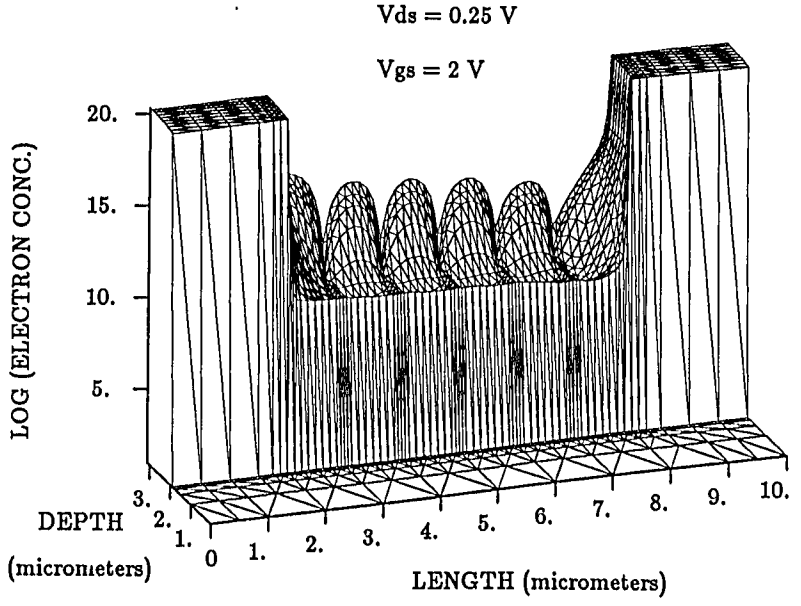

Fig. 4. *Electron concentration within the simulated polycrystalline-silicon MOSFET:* V_{GS} = *2.0 V,* V_{DS} =*0.25 V.*

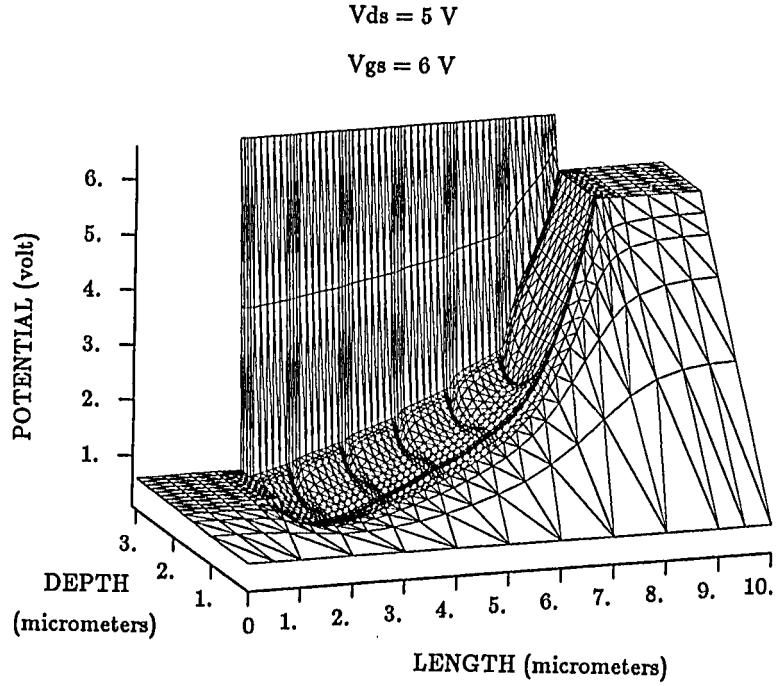

Fig. 5. *Electric potential within the simulated polycrystalline-silicon MOSFET:* V_{GS} = *6.0 V,* V_{DS} =*5.0 V.*

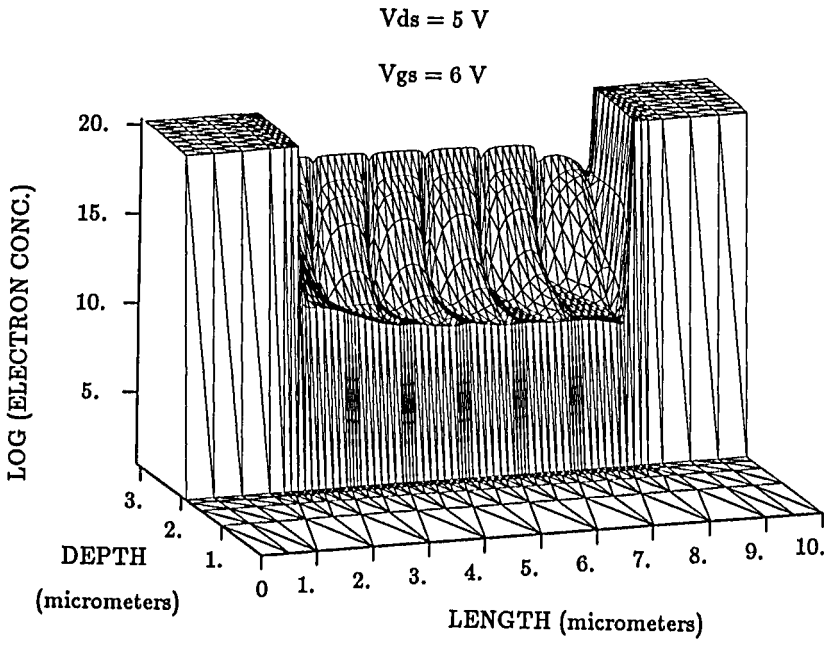

Fig. 6. *Electron concentration within the simulated polycrystalline-silicon MOSFET:* V_{GS} = *6.0 V,* V_{DS} =*5.0 V.*

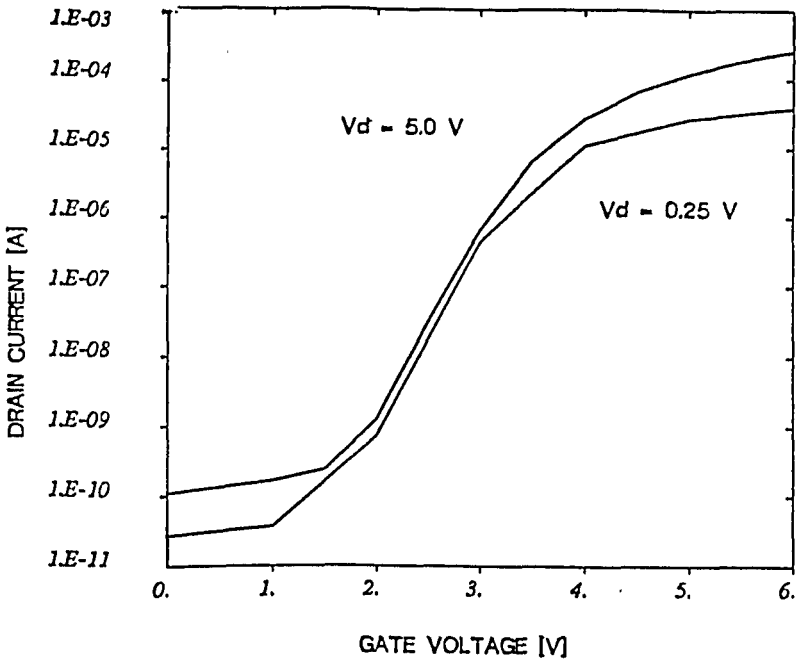

Fig. 7. *Simulated turn-on characteristics of the polycrystalline-silicon MOSFET. The selected V_{DS} values are 0.25 and 5.0 V.*

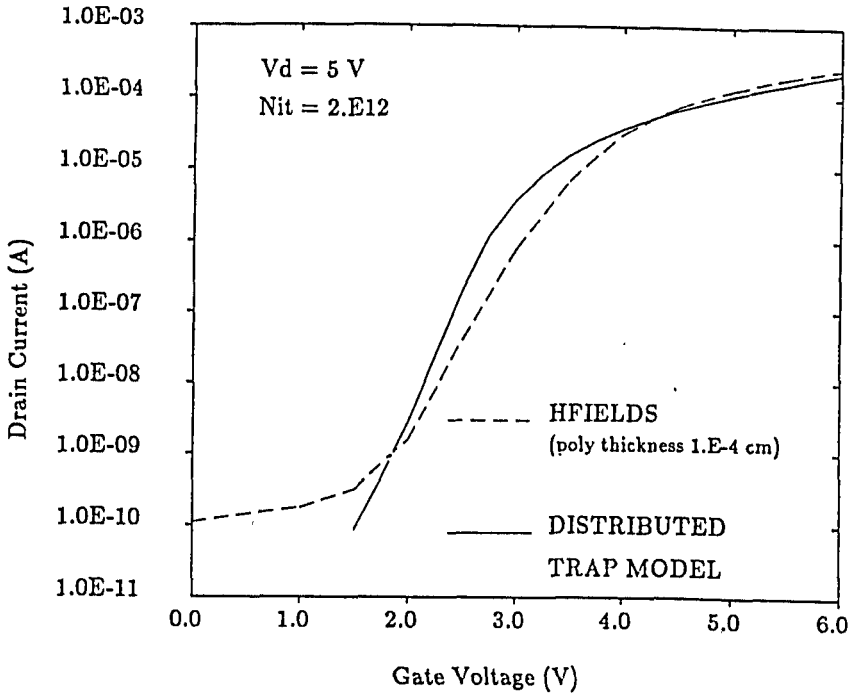

Fig. 8. *Simulated turn-on characteristics of the 1 μm-thick polycrystalline-silicon MOSFET against distributed-trap model.*

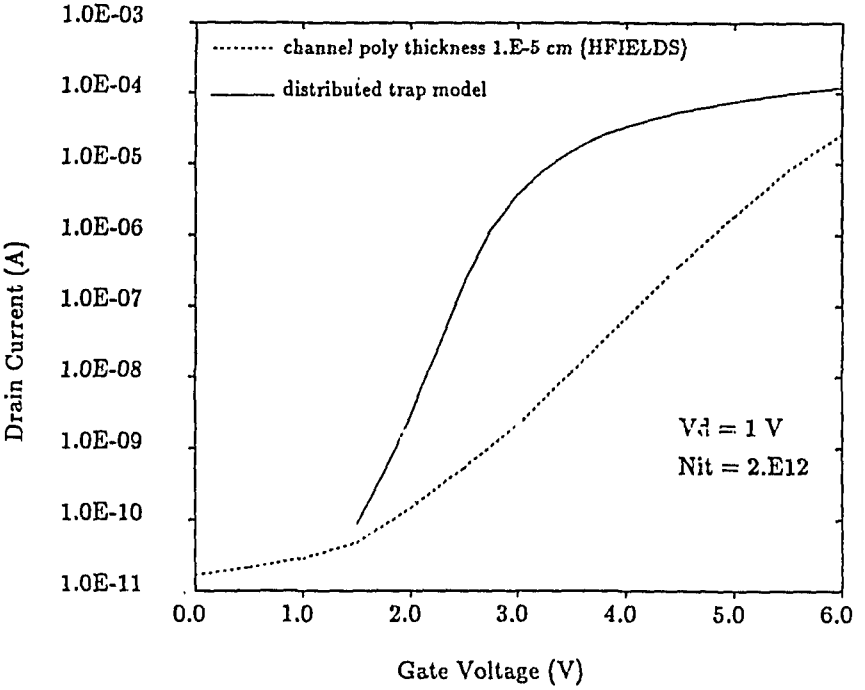

Fig. 9. *Simulated turn-on characteristics of the 0.1 μm-thick polycrystalline-silicon MOSFET against distributed-trap model.*

Fermi level at both $Si - SiO_2$ interfaces. Device transconductance in strong inversion very nearly equals the theoretical value $(W/L)\mu C_{ox} V_{DS}$. In order that the MOSFET turns on, it is necessary to fill all electron traps. After this condition is met, any further increase in gate potential enhances the channel conductance. Consequently, the device transconductance is not substantially influenced by monovalent traps located at midgap. The turn-on characteristics obtained with the bulk-distributed trap model are compared with HFIELDS simulation results in figure 8. The two curves are very close in strong inversion, but deviate somewhat in subthreshold conditions, where the barriers experienced by channel electrons are not properly accounted for by the distributed-trap model. The crossing of the curves near $V_G = 2V$ is due to generation currents which are neglected by the simplified model. Figure 9 compares the turn-on characteristics of the 0.1 μm-thick transistor with the simplified model. Very large deviations occur in any region of operation, indicating that the assumed boundary condition at the bottom-insulator interface is not adequate in this case.

Finally, we have investigated the influence of the boundary condition imposed at the bottom plate of the thick oxide. Figures 10 and 11 show the electric potential for the 0.1 μm-thick transistor, using Dirichlet and Neumann boundary conditions, respectively. In spite of the different potential distribution in the thick oxide, the resulting turn-on characteristics are very nearly identical, as shown in figure 12.

5. Conclusions

From our simulation results, a few conclusions can be drawn on polycrystalline-silicon MOSFET operation:

- The large threshold voltage experimentally observed in enhancement mode transistors can only be justified by assuming the simultaneous existence of both acceptor and donor states at the grain boundary [7]. This conclusion is consistent with the

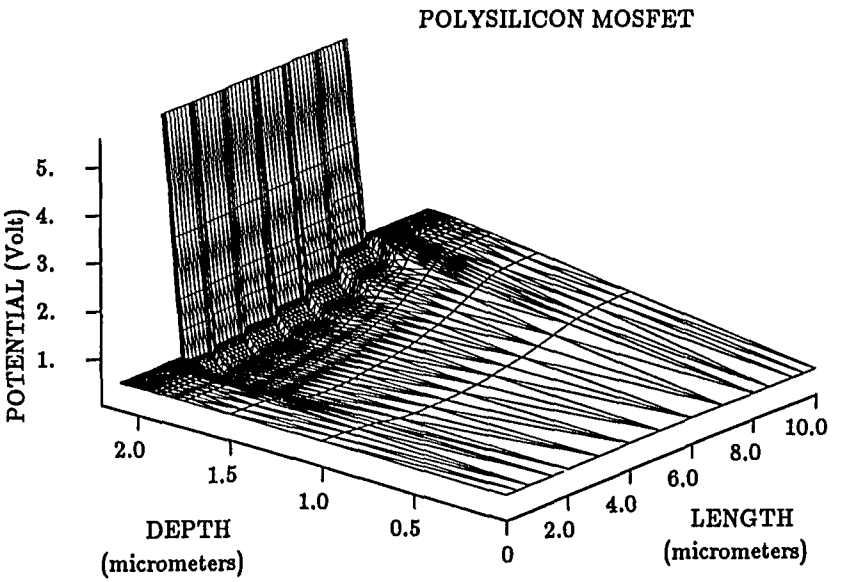

Fig. 10. *Electric potential within the 0.1μm-thick polycrystalline-silicon MOSFET using Dirichlet boundary conditions at the bottom-plate of the back insulator.* V_{GS} = *5.0 V,* V_{DS} =*1.0 V.*

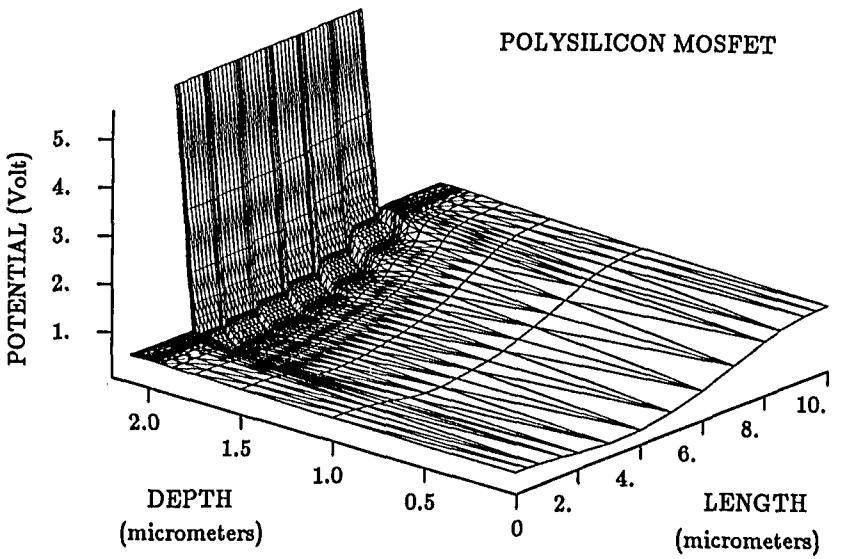

Fig. 11. *Electric potential within the 0.1μm-thick polycrystalline-silicon MOSFET using Neumann boundary conditions at the bottom of the back insulator.* V_{GS} = *5.0 V,* V_{DS} =*1.0 V.*

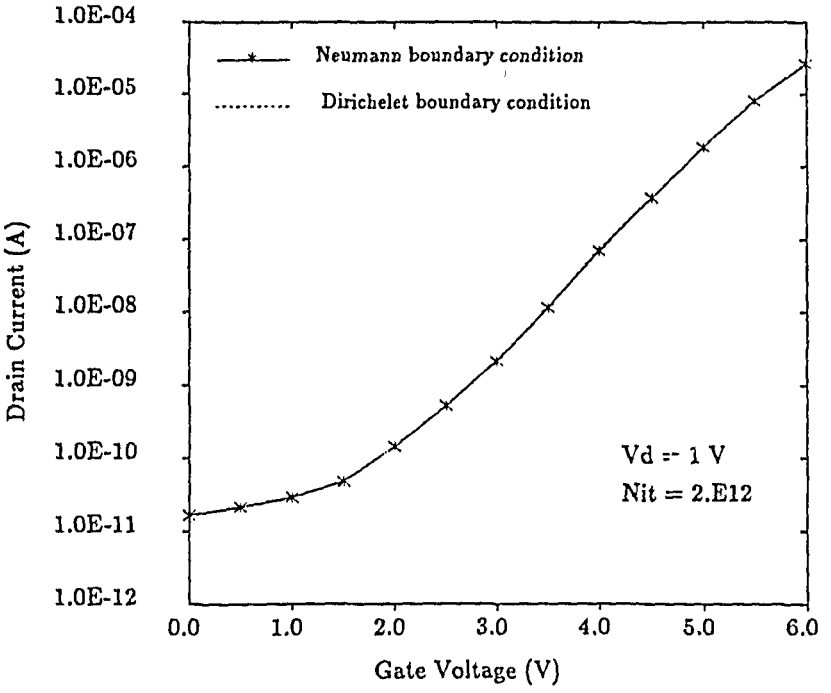

Fig. 12. *Simulated turn-on characteristics for the 0.1μm-thick MOSFET using Dirichlet and Neumann boundary conditions. No appreciable difference can be noticed.*

generally-agreed result that grain boundaries basically behave as majority-carrier traps.

- The slope of the turn-on characteristics can be related to the nature of interface states: more specifically, monovalent states located at midgap influence mostly the threshold voltage but, once inversion is reached at the grain boundary and all traps are filled, any further increase in gate voltage will substantially enhance the channel conductance. On the other hand, a continuous energy-distribution of interface states will never lead to a complete saturation of the traps, thus resulting in reduced transconductance.
- The current increase experimentally observed at negative gate voltages [1,2], cannot be justified by our purely electrostatic model: no highly-conductive channel is formed at the back-oxide silicon interface even at large negative gate voltages.
- Generation currents based on pure thermal emission are very limited and do not appreciably contribute to the leakage current. Therefore, the main physical origin of leakage is related to the existence of conduction paths along grain boundaries and the back-oxide silicon interface, where the semiconductor is very nearly intrinsic.
- Current increase at negative gate voltages can be traced back to either field-enhanced generation at grain boundary traps, or to impact ionization. Neither effect was incorporated in our simulations, so that we cannot identify the major source of such an increase.
- The use of a simplified model based on an equivalent number of bulk-distributed traps provides reasonable results only if the semiconductor thickness is large enough to justify an asymptotic boundary condition at the bottom-insulator interface, and in strong-inversion conditions. For thin-film transistors, the simplified model is totally unreliable.

In conclusion, we have shown that-numerical device simulation represents a useful tool

for a better understanding of thin-film transistors. Grain boundaries in polycrystalline silicon influence the device performance in a rather unpredictable fashion, thus making numerical analysis an essential tool for clever designs of such devices. The general structure of our simulation program has easily allowed us to incorporate the effect of traps at the grain boundaries and at $Si - SiO_2$ interfaces into the numerical model.

It is believed that, once the basic physical mechanisms affecting device behavior are unambiguously identified and incorporated in the code, numerical-device simulation will become an effective design tool for polycrystalline silicon devices as it is now for single-crystal devices.

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