Performance Optimization and Assessment of normally-on $Ga_{0.47}In_{0.53}$ As Injection FET's

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Summary:

The small signal performance of normally-on submicronic gate Ga In As injection FET's as a function of channel length is assessed using a two-dimensional energy model incorparating non-stationary electron dynamics. The results of the simulation indicate that for 0.3 um gate, short channel FET's, intrinsic cut-off frequencies as high as 80 GHz can be reached together with a transconductance of 180 mS/mm making Ga In As FET's a prime contender for millimetric frequency low-noise amplification.

1. Introduction:

It is common knowledge that the velocity of the electrons under the gate of submicronic gate Ga As MESFET's can reach velocities much higher than expected from the quasi-stationary velocity-field characteristics of Ga As. This phenomenon commonly known as velocity overshoot result from the finite time required by the cold electrons injected in the high field region under the gate to acquire sufficient energy to be transferred to the low mobility satellite valleys and the finite scattering rate by the longitudinal optical phonons that ensure the transfer. During this time, the electrons are subjected to large fields that can exceed 100 KV/cm and result in velocity peaks exceeding 4×10^7 cm/s [1]. A simple analysis by Salmer et al. [2] showed that the cut-off frequency of submicronic FET's is proportional to the product of the low-field mobility by Γ-L valley energy separation. In that respect

Ga In As (lattice matched to In P) holds a pronounced advantage over Ga As and In P. In fact, for a doping concentration of $10^{17}cm^{-3}$, its low-field mobility is around 7900 $cm^2/V.s.$ compared to 4600 and 3100 for Ga As and In P respectively. Similarly its Γ-L valley separation while comparable with that of In P is 66% higher than that of Ga As. Beside its superior transport properties, Ga In As is used in integrated PIN-FET optoelectronic receivers for long wavelength optical fiber communication systems on account of its convenient bandgap.

2. Ga In As FET Structures:

In spite of its remarkable transport properties the small band gap of Ga In As (0.75 eV) forbids the use of Schottky barrier gate structures on account of the large leakage gate current resulting from the small barrier height (0.2 eV). Moreover this small band gap make Ga In As FET's prone to channel breakdown if large stationary domains are to form (as in Ga As MESFET's). Thus different gate configurations had to be investigated. These can be categorized in three main structures:

(i) Insulator assisted Schottky barrier gates.

(ii) Heterostructure assisted Schottky barrier gates.

(iii) P-N Junction gates.

The first type of gates consists of an inversion mode MIS structure where a 100-300 A° thick Si_3N_4 insulating layer contributes to raising the barrier height above 0.5V. [3-4].

The second type consists of a thin layer (about 600 A° thick) of a large band gap material such as $Al_{0.48}\ In_{0.52}\ As$ inserted between the Ga In As channel and the metal gate [5]. The resultant Schottky barrier is higher than in the previous type (0.8 V) whereas the transconductance is smaller.

These two gate structures suffer from the same problems namely a large drain conductance, failure to reach complete pinch off and current drifting due to the presence of interface states.

The third type of gates consists of a P-N junction with the P side being a thin and heavily doped (10^{18} -10^{19} cm^{-3}) layer usually obtained by MBE although ion implantation was also used [6-7]. However for relatively large channel dopings ($> 10^{17}$ cm^{-3}),

the leakage current of the gate was found to be two orders of magnitude higher than in the case of lightly doped channels (most probably due to tunneling). One the other hand in the last case, the drain current was lower. In general junction gate seem to be promising if we could reconcile the requirement of a low leakage current and a reasonable drain current.

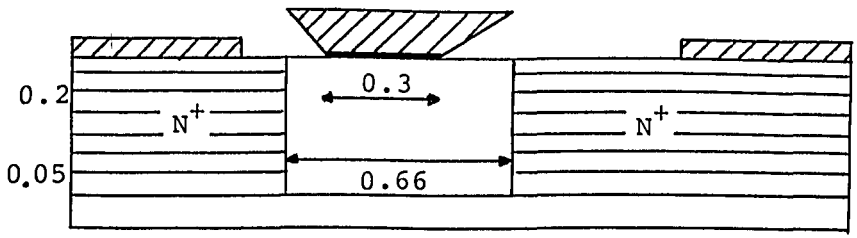
This can achieved through the use of an injection FET structure which consists of a lightly doped channel sandwiched between two heavily doped n^+ regions. Electron injection over the n^+- n^- diffusion barrier on the source side ensures the supply of extra electrons to the channel. In the same time, the high overshoot velocities attained by the electrons on account of reduced scattering by ionized impurities act to increase the current.

In general the closer the n^+regions to the gate, the higher the current and the transconductance but also the higher the gate-to-source capacitance. Thus as for as the cut-off frequency is concerned ($f_t = \frac{g_m}{2\pi C_{gs}}$) an optimum position exists.

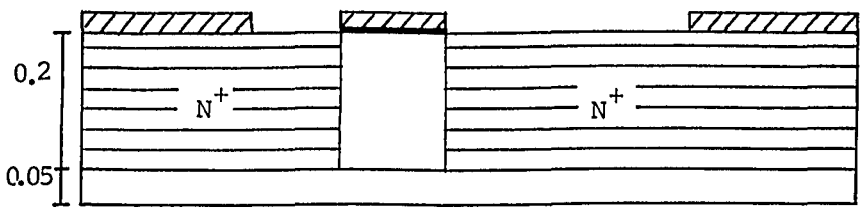
Thus our purpose here is to obtain an accurate quantitative assessment of the performance of submicronic Ga In As injection FET's for different values of channel length through the use of an appropriate numerical modeling technique.

3. Device Modeling:

The structural features of the devices modeled are shown in fig. (1). It is seen that the two devices analyzed differ only in channel length. As the saturation velocity of Ga In As is lower than that of Ga As only Ga In As FET's with submicronic gates can present an advantage over Ga As ones. Furthermore as these FET's are meant to operate at millimetric frequencies a gate length of 0.3 um was chosen. The channel doping was taken $10^{16}cm^{-3}$ as lower doping levels,would decrease the current significantly while the corresponding increase in low-field mobility is limited as alloy scattering is independent of doping concentration. The doping of the n^+regions was limited to $2x10^{17}cm^{-3}$ for computational convenience. In device I the channel length was 0.66 μm whereas in device II, the channel length equalled the gate length (0.3 μm). It should be noted that the realization of device I requires a special gate self-alignement technique developed by Ismail and Beneking [8] whereas device I can be implemented using the SAINT technology [9].



(a)



(b)

Fig. 1 Structural features of devices simulated
(a) Device I. (b) Device II.

Device simulation was carried using a two-dimensional, finite difference, energy model developed by Ibrahim [10]. The model is based on the particle, momentum and energy conservation equations derived by Blotekjaer [11] from Boltzaman transport equations. By averaging out the charge density, the momentum and the energy over the different valleys, we define an equivalent single electron gas, the state of which is solely dependent on the average local energy of the electrons. Thus the effective mass (m) the mobility (u), the electronic temperature and the energy relaxation time are considered to be energy dependent instead of field dependent as in local models. The energy dependence of these parameters obtained from the results of M.C. simulations incorporating alloy scattering. This finally leads to the following set of coupled equations

$$\nabla^2 V = \frac{q}{\epsilon}(n - N_d) \qquad (1)$$

$$q\frac{\partial n}{\partial t} + \nabla . \underline{J} = 0 \qquad (2)$$

$$\underline{J} = \mu(\zeta)\left\{ qn\,\underline{V} - \underline{\nabla}\,[kT(\zeta)n]\right\} \qquad (3)$$

$$\frac{\partial(n\zeta)}{\partial t} = \frac{1}{q}\underline{J}.\underline{E} - \frac{1}{q}\nabla .[kT(\zeta)\underline{J}] - \frac{1}{q}\nabla .(\underline{J}\zeta) - n\left(\frac{\zeta - \zeta_0}{\tau_\zeta}\right) \qquad (4)$$

where
- n is the charge density
- J is the current density
- V the potential
- E the electric field
- μ the mobility of the equivalent electron gas.
- T the temperature of the equivalent electron gas.
- τ_ζ the energy relaxation time.
- ζ the average electron energy.

Poisson's equation is solved directly using the method of Choleski whereas the continuity and energy relaxation equations are solved by the S.O.R. method using a semi-implicit formulation.

4. Simulation Results:

4.1 Charge, Potential and Energy distributions

Fig2(a,b,c) and 3(a,b,c) give the constant charge,

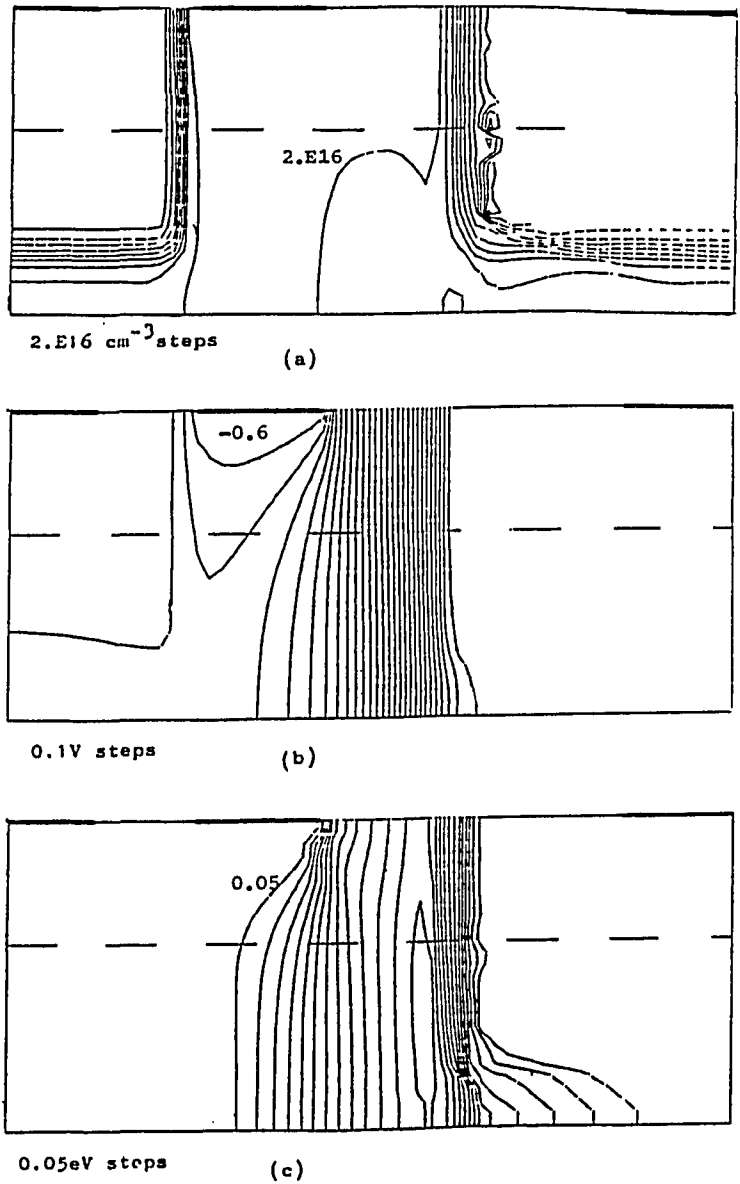


Fig. 2 (a) Constant charge. (b) Contant potentral and (c) Constant energy contours for device I at V_{gs}= 0 and V_{ds} = 2V.

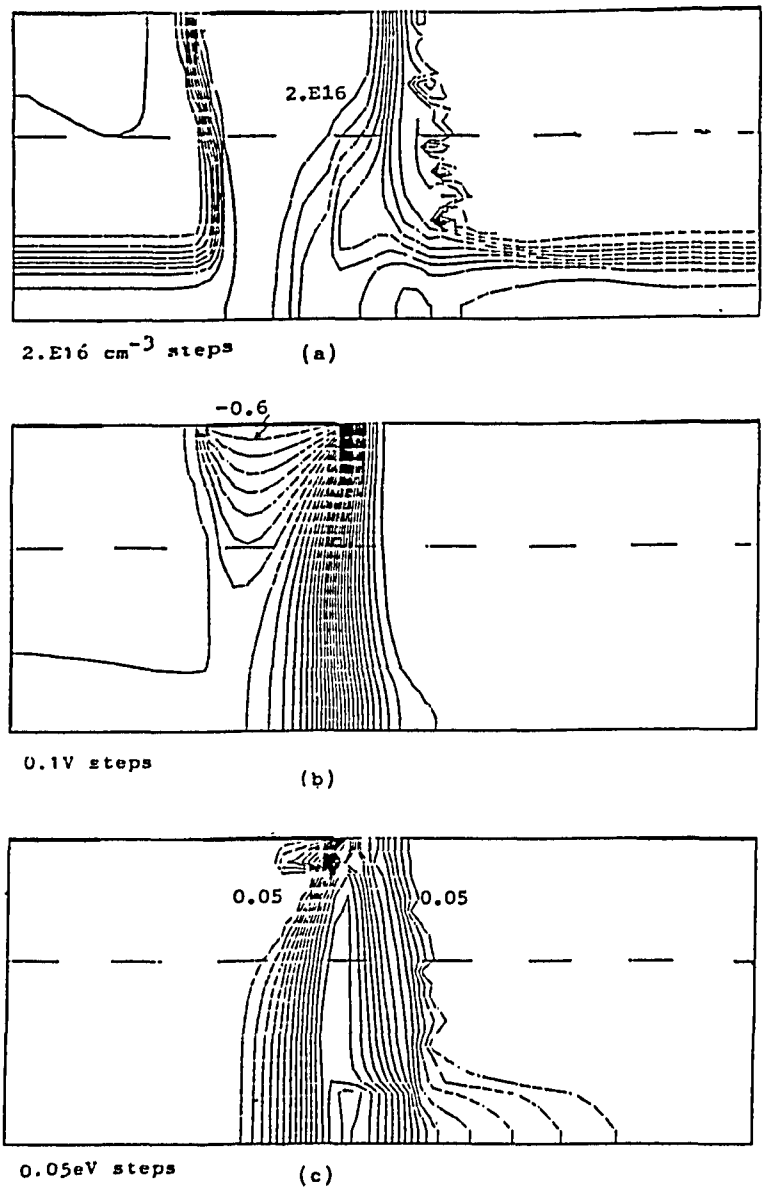


Fig. 3 (a) Constant charge. (b) Constant potential and (c) Constant energy contours for device II at V_{gs} = 0 and V_{ds} = 2.5V.

potential and energy contours for device I and device II respectively for $V_{gs}=0$.

The constant charge density contours (2a) and (3a) show that injection becomes more pronounced in regions away from the gate. It is also more important in the case of device II on account of the proximity of the n^+region on the drain side. Fig. (4) shows the longitudinal distribution of the charge density 0.2 um below the gate at zero gate bias for the two devices where it is clearly seen the difference in charge concentrations. A special feature of the charge distribution in device II is the presence of a small accumulation region below the drain edge of the gate.

The equipotential contours in device I are all practically confined to the region between the drain edge of the gate and the n^+ region and is more or less uniformly distributed. In device II the proximity of the n^+ regions to the gate result in large electric fields that can reach 150 Kv/cm. This difference in potential distribution in both devices reflects on the energy distribution. In device I the maximum energy is reached at a position approximately 0.2 um beyond the drain edge of the gate whereas in device II it occurs at the drain edge of the gate just as in conventional Ga As MESFET's.Fig. (5).shows the longitudinal distribution of the longitudinal velocity and the energy 0.2 μm below the gate indevice I. It should be noted that the peak velocity attained, is 1×10^8 cm/sec and occurs below the drain edge of the gate. The average velocity of the electrons below the gate was found to be 6×10^7 cm/sec. Beyond the gate, velocity undershoot takes place. Fig.(6)shows the same distributions for device II. Although the peak velocity here is higher by 20%, the average velocity under the gate is only 8% higher than in device I(6.5×10^7 cm/sec) as the peak velocity occurs under the middle of the gate. It should be noted however that the actual peak velocities should be smaller as we have neglected in the momentum relaxation equation (eq.3) the term incorporating the effect of the spatial gradient of momentum. If taken into consideration the longitudinal distribution of the velocity would be less peaky and the maximum reduced by as much as 25%. The average velocity however would not be significantly affected.

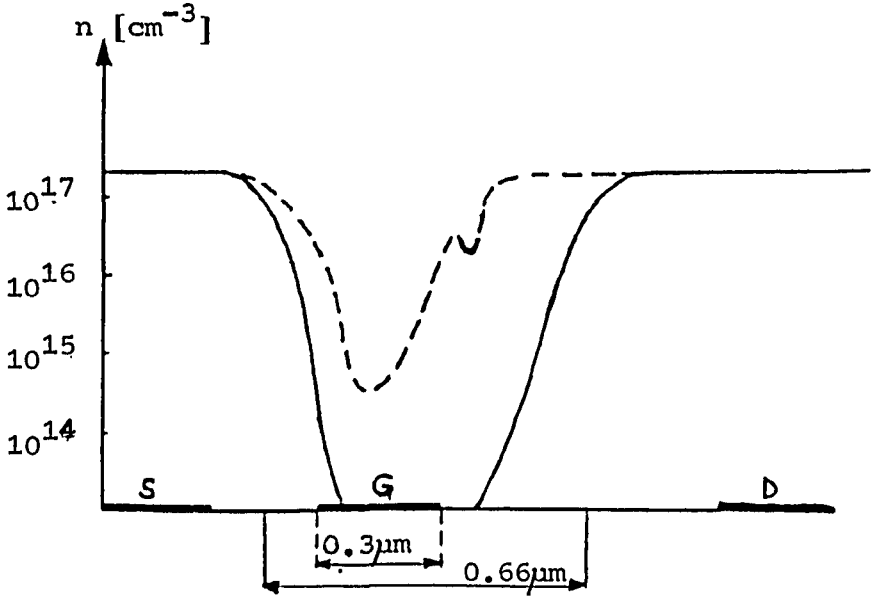


Fig. 4 Longitudinal charge density distribution 0.2 um below the gate for V_{gs}= 0 and V_{ds}= 2.5V.

——— Device I ----- Device II

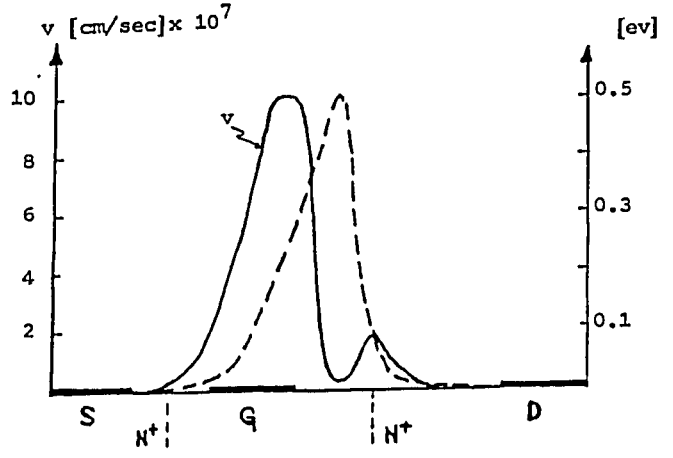


Fig. 5 Longitudinal distributions of energy and velocity 0.2 um below the gate of device I (V_{gs}=0, V_{ds}=2.5V).

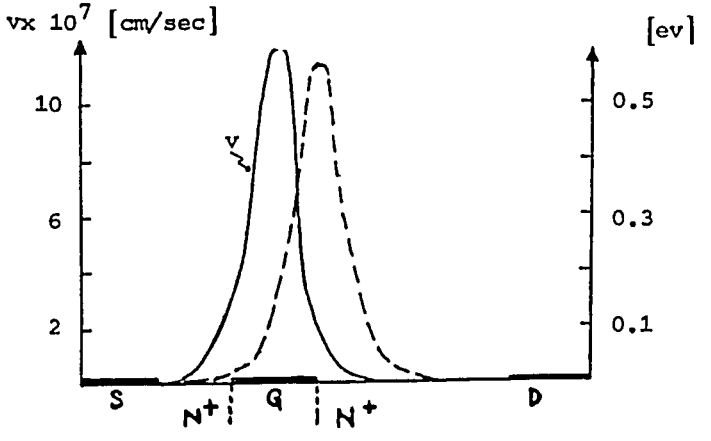


Fig. 6 Longitudinal distributions of energy and velocity 0.2 um below the gate of device II (V_{gs}= 0 , V_{ds} = 2.5V).

4.2 I-V characteristics:

The output current characteristics of both devices are shown in fig. (7) and (8). Because of the absence of any sizeable domain, which is usually responsible for current saturation in conventional Ga As FET's, the transistor currents show no saturation until V_{ds} = 2.5 V. This aspect is more pronounced in device II as the drain voltage is more effective in lowering the n^+-n diffusion barrier. However the current in device II for V_{gs} = 0 and V_{ds} = 2.5 V is more than five times the current in device I. This increase is mainly attributed to increased charge injection in the channel, the difference between average velocities being rather small. As for the pinch off voltages, they are -1V and -3V respectively.

4.3 Small Signal Parameters:

The evolution of the small signal parameters of the two devices with gate bias is shown in fig (9) and (10). At zero gate bias, the transconductance of the second device is seen to be quite large compared to that of the first device (180 mS/mm versus 74 ms/m). The ratio of transconductances is seen to be much smaller than the current ratio. This is due to the fact that the current control mechanism is different from that of a conventional FET. It should be noted that g_m is found to be an increasing function of the drain voltage V_{ds} while in Ga As conventional MESFET's, the transconductance variation with V_{ds} usually exhibit a peak around the knee voltage and then drops slowly with voltage. This is a domain related feature [12] which does occur in injection FET's due to the absence of domains.

The gate-to-source capacitance is also evidently higher in device II than in device I. However C_{gs} drops with V_{gs} more slowly than the transconductance. Thus the cut-off frequency ($f_t = \frac{g_m}{2\pi C_{gs}}$) will drop with V_{qs}. For device II it will vary from 80 GHz at V_{gs} = 0 to 45 GHz at V_{gs} = -1.5V. Whereas in device I it drops from 60 GHz at V_{gs} = 0, to 45 GHz at -0.25 V.

The absence of domain is also felt in the large value of drain conductance specially in device II. In both devices however, as long as V_{gs} is away from pinch off, the drain conductance varies little with V_{gs}.

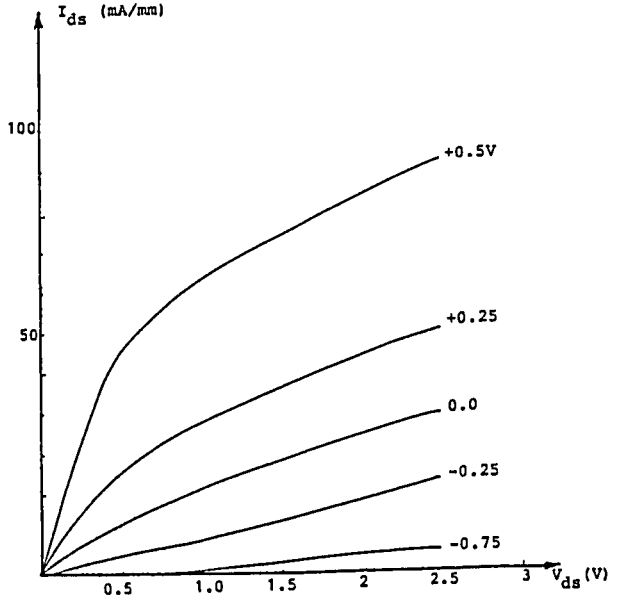


Fig. 7 I_{ds} - V_{ds} Characteristics of device I.

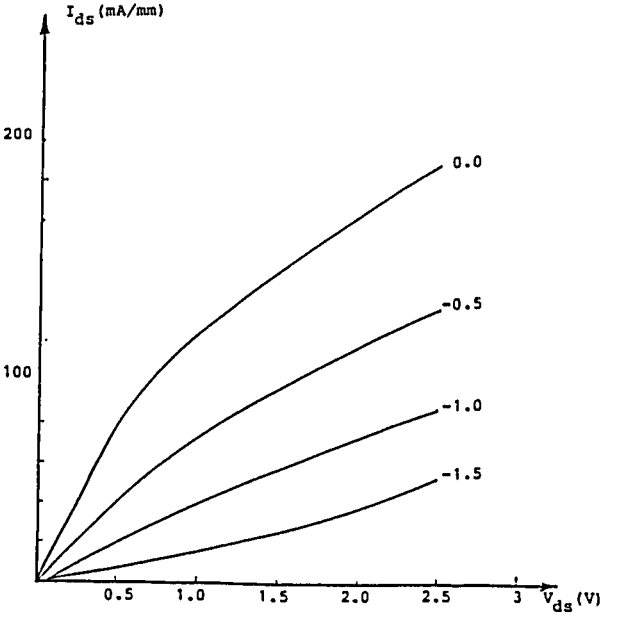


Fig. 8 I_{ds} - V_{ds} Characteristics of device II.

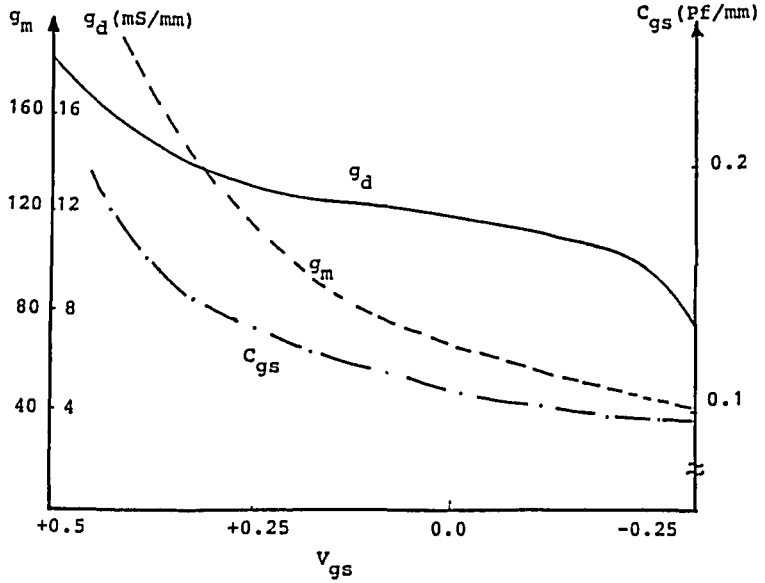


Fig. 9 Small signal parameters of device I

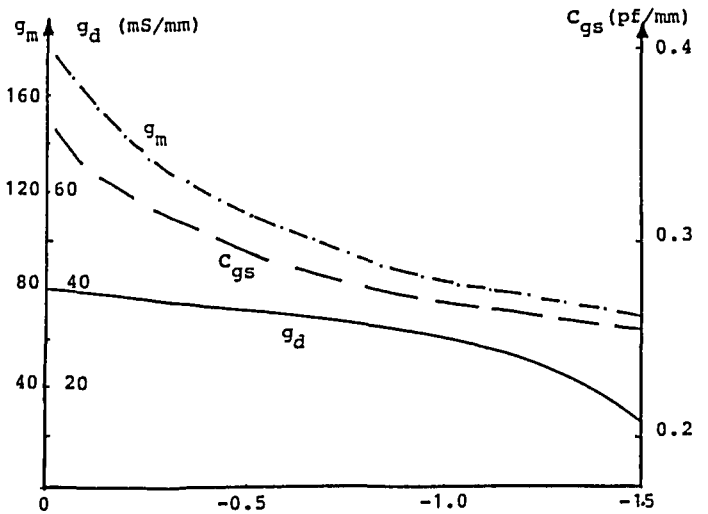


Fig.10 Small signal parameters of device II

As the noise figure at millimetric frequencies is proportional to the factor $\sqrt{1+(\frac{wC_{gd}}{g_d})^2}$, [13] the ratio of C_{gd}/g_d becomes quite important. In fact this factor contributes an extra 1.5 db to the noise figure of device II at 37 GHz whereas this same contribution occurs at 20 GHz for device I.

Table 1 summarizes the performance of the two devices at V_{gs}= 0, V_{ds} = 2.5 V and compares it with that of a conventional planar Ga As MESFET with a channel thickness of 0.1 um doped to $2x10^{17}cm^{-3}$ and having the same structural parameters as the Ga In As FET's

Table 1

	Ga As MESFET	Ga In As Injection FET	
		Device I	Device II
I_{ds} (mA/mm)	280	40	206
V_p (V)	-2	-1	-3
g_m (mS/mm)	240	74	180
g_d (mS/mm)	10	12	40
C_{gs} (pf/mm)	0.56	0.2	0.32
C_{gd} (pf/mm)	0.007	0.009	0.017
f_t (GHz)	68	59	80
C_{gd}/g_d (ps)	0.7	0.75	0.43
g_m/g_d	2.4	6.2	4.5

5. Conclusion:

From the above results it is seen that short channel Ga In As injection FET's can reach higher cut-off frequencies and lower noise figures at millimetric frequencies than Ga As MESFET's together with reasonable drain currents and transconductances. It should be kept in mind that further optimization is still possible by varying the doping of the regions and the use of Al In As buffer layer for charge confinement thus making better performances possible providing the current technological problems are resolved.

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