MONTE-CARLO SIMULATION OF THIN FILM DEPOSITION IN A SQUARE GROOVE

M J Cooke

University College Swansea, Singleton Park, Swansea SA2 8PP, United Kingdom

1   ABSTRACT

A Monte-Carlo programme has been developed to simulate thin film deposition in a square groove. It demonstrates that conformal coating requires (1) the mean free part to be greater than the feature size; (2) a low sticking coefficient for incoming reactant molecules.

2   INTRODUCTION

The increasing use of anisotropic etching in the manufacture of integrated circuits is stimulating research into methods of coating steep-walled surface structures uniformly. The problem is particularly acute in the case of metal deposition, where thin portions are likely to lead to early failure. Technical solutions include planarization, bias sputtering, and chemical vapour deposition (CVD).

Numerical and theoretical studies of both deposition and etching have been published which include evaporation step coverage[1], sputtering uniformity[2], general algorithms[3] and thermodynamic analysis[4]. The most common approach has been to set up an initial geometry and to compute a new surface profile point by point by considering the relative orientations of source and surface element. Motion in the gas phase is assumed to be either diffusive or collision-free, a sticking coefficient of unity is used, and surface mobility is neglected in all cases but one[3]. Where a

plasma or energetic beam is present the angular variaton of etch/deposition rate has been considered for both physical and chemical processes. These analyses neglect two interacting cases:

(1) The transition from collision-free to diffusion-dominated gas phase motion.

(2) the effect of a non-zero sticking coefficient on step coverage.

The mean free path λ varies with gas pressure p:

λp = constant $\approx 7 \times 10^{-3}$ m.Pa for air. (1)

For atom clusters and large molecules the constant could be smaller by up to an order of magnitude, making λ of order 10^{-6}m at pressures 10^3-10^4Pa. In some reduced pressure CVD systems therefore, the reactants could be considered to move by gas flow and diffusion only several λ from a stepped surface. Near the surface neither diffusion nor collision free motion hold good.

The second case can be posed as a question: to what extent is the conformal coating often obtained by CVD due to a rate-limiting step on the surface? A small sticking coefficient means that the walls and floor of a groove act as sources for reactant molecules, so that conformal coating might be caused by the efficient re-distribution of reactants rather than the slow decomposition of molecules on a fully loaded surface. A Monte-Carlo method was chosen as the simplest and most flexible approach to these problems.

3   SIMULATION

The problem domain is illustrated in Figure 1. Deposition was recorded only in the central section around the groove, while the outer sections allowed the floor of the groove to view the full intensity of the source.

Molecules are introduced at or near the top boundary with a random starting point and direction. Straight line motion is used, with the following boundary conditions:

(1) Specular reflection at the left and right sides.

(2) Re-introduction with a random direction from the exit point at the top.

(3) Either sticking or random angle desorption from the substrate.
NAG library routines are used to supply random numbers where required.

Collisions are handled by selecting a random number n $0<n<1$ and comparing it with the collision probability P in the distance R to the substrate or domain boundary.

$$P = 1 - exp\ (-R/\lambda)$$
$$n \leqslant P \qquad collision$$
$$n > P \qquad no\ collision$$

If there is a collision a new random direction is taken after a moving distance L in the original direction:

$$L = -\lambda ln(1-n) \qquad\qquad (2)$$

The simulator also permits variable surface mobility. In the results presented here this is not used, save to prevent the formation of filaments by forcing new deposition sites to have at least two occupied neighbour sites (from eight).

The effect of deposition rate is accounted by storing deposition sites in a temporary buffer and transfering them into the main geometry array in batches. A small buffer corresponds to a low deposition rate.

In all the results presented here a one micron square groove was used with new molecules appearing $5\mu m$ above the plane surface. The mean free path λ and the sticking coefficient s $0<s<1$ were varied. The groove width was taken to be 100 deposition sites wide. Run on an ICL2900 series machine, the code used between .02 and 2 seconds of CPU time per sample, depending strongly on the parameters chosen.

4   RESULTS

Figure 2 shows a typical result after 8000 trials. Only 26% of the trials result in deposition within the recorded zone: 70% are deposited in regions 2 and 3 while 4% are lost through programme traps, mainly double occupation of a deposition site. The film contains about 7% voids, not shown in the figure. Figure 3 details the development of this simulation. The ratio of (groove floor thickness)/(top surface thickness) appears to converge reasonably well. True convergence is not expected, because the growing film will shadow the groove floor increasingly, causing the ratio to fall. The left-right asymmetry is also shown in Figure 3, and is not so well behaved. The reason for this is not clear at present: it is believed that the programme introduces no such bias, so a test with an alternative random number generator is indicated. Symmetry could, of course, be imposed in the programme by mirroring deposition about the centre line.

Table 1 summarises the main results. Contrary to popular belief, decreasing the mean free path below the size of the surface feature has a deterious effect on coating conformity. It is interesting to note, however, that the mean free path does have to fall well below the feature size before any adverse effect is seen. Most LPCVD equipment is safe on this score, and will become better as dimensions shrink. The trend towards conformal coating as the sticking coefficient is reduced is clearly shown.

Table 1

Sticking coefficent = 1	1 micron square groove		
Mean free path λ m:	10^{-4}	10^{-6}	3.10^{-7}
Groove floor thickness / Top surface thickness	0.26	0.26	0.12

Mean free path = 10^{-4}m	1 micron square groove		
Sticking coefficient:	0.1	0.5	1.0
Groove floor thickness / Top surface thickness	0.72	0.38	0.26

5 DISCUSSION

The main finding of this study is the confirmation that a low sticking coefficient enhances step coverage while low mean free path leads to poor step coverage. Each area element on the plane surface, including the area of the groove, views the same intensity source. For the case of a square groove, the source has to coat three times the surface area within the groove (compared to unit area on the plane surface), so a film about one third as thick is deposited if the sticking coefficient is unity. Conformal coating therefore requires transport of material into the groove region. A low sticking coefficient causes this, because the material entering the groove is likely to make multiple surface impacts within the groove before possibly desorbing back into the bulk of the gas, where a single desorption does the same thing on the plane surface.

This work leaves open the cause of a low sticking coefficient. It could be that the deposited material intrinsically has a low sticking coefficient, or that sites occupied by unreacted absorbed molecules reject further arrivals, while vacant sites accept them. It is planned to simulate this aspect in the next phase of the study.

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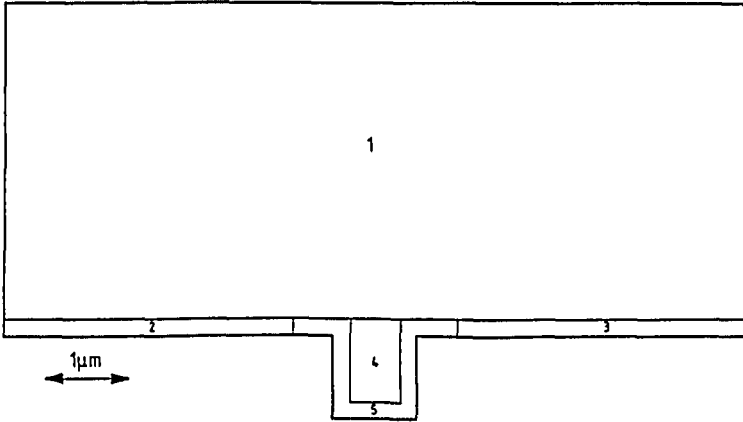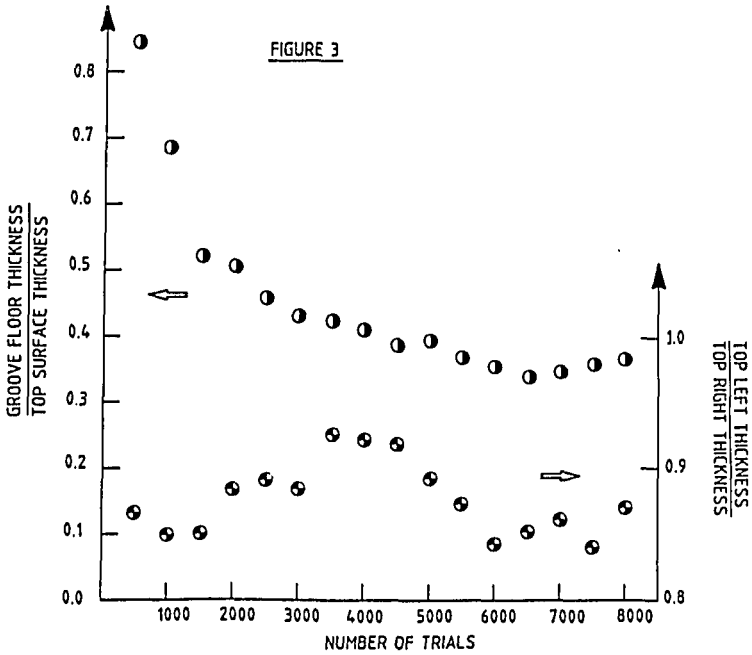   J. Appl. Phys. 57, 929-942, 1985.

FIGURE 1

FIGURE 3

$\lambda = 10^{-4}$ m
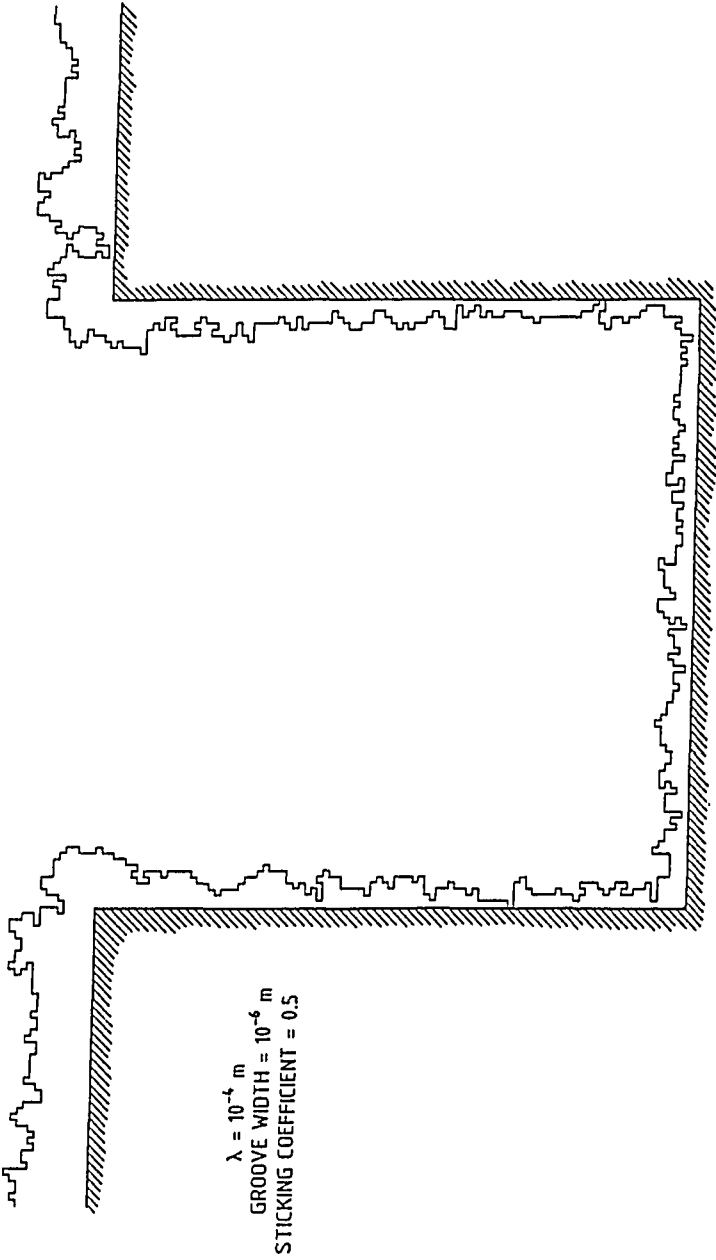GROOVE WIDTH = 10^{-6} m
STICKING COEFFICIENT = 0.5

FIGURE 2

CONTROL OF OXIDE GROWTH BY REAL-TIME SIMULATION

E. Cameron, J. Robertson, R. Holwill

Edinburgh Microfabrication Facility, University of Edinburgh.

SUMMARY

As critical device features are reduced in size, it
becomes increasingly important to control the uniformity and
reproducibility of the critical layers which determine device
performance.   The gate oxide is one such layer, and this
paper outlines a technique which has been developed to provide
more direct control of oxide growth by taking into account all
the major process variables encountered during the growth
process.   Data available through the growth furnace digital
process controller is supplied to a growth simulation program
which is used to control the time the wafers spend in the
furnace.   Results are presented for a wet oxidation process
which involves oxide growth under non-steady-state conditions.

1. INTRODUCTION

Computer simulation of semiconductor process is an
important tool in process development. By allowing 'what if'
analysis over a variety of fabrication steps, simulation can
save costly and time consuming experimentation.   However,
as models become refined and more accurate, simulation need
not be limited to only this role.   This paper considers an
application where a conventional negative feedback control
loop has been replaced by a simulation model. Providing the
whole system response is slow compared with trial time of the
simulator, many system variables can be continuously monitored
and used as inputs to the simulator.   The simulated results
may then be used to provide real-time control and to predict
process end points.

The chosen application is thermal growth of thin silicon
dioxide films.   The oxide thickness appears as a first order
term in all principal MOS device equations.   As features in
VLSI circuits are reduced, thinner oxides are required as shown

in Table 1. Growth times may be reduced, but transient
effects become progressively more important and conventional
oxidation control systems are not sufficient to maintain
thickness tolerances.

Table 1

Min Device Feature (μm)	Gate Oxide Thickness (Å)	Required Tolerance (Å)	Dry Oxidation time at 950°C (min)
5	800	40	245
2.5	400	20	90
1.25	250	12.5	40
0.5	100	5	9

2. CONTROL OF OXIDE GROWTH

If improved control of oxide growth is to be achieved
the causes of thickness variability should be separately
examined. If the mechanisms are independent, they may be
controlled separately. The main factors are:

i) Variations within a single batch of wafers

These are usually due to furnace 'individuality' and
factors such as non-uniform temperature caused by a hydrogen
torch or the effective increase in oxidation based on the
first-in/last-out principle. If this variation is to be
reduced, it would require changes to furnace hardware and this
is not considered here.

ii) Batch-to-batch variation

This is present because furnace treatments are not
completely reproducible, despite elaborate digital control
systems. The basic mechanism for furnace control is a neg-
ative feedback loop (Fig 1), which attempts to maintain a
constant temperature. Other loops control the remaining fur-
nace variables: gas flows and boat position. Assuming that
these control loops are well-behaved, ie that deviations
from set-point are small, then control of oxide thickness may
be achieved with accurate process timing. Characteristic
oxide growth curves at different temperatures are frequently
used to predict the oxidation time for any specified thick-
ness.

However, temperature disturbances frequently occur - for
example by loading cold wafers into a furnace at 950°C. The
temperature controller responds, but requires a period of
time to fully recover to its set-point temperature. This has
an influence on oxide thickness which is not assessed in oxide
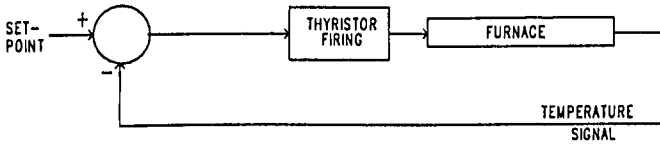growth curves, and results in variations between furnace

Figure 1
Negative Feedback in Temperature Control

treatments. Likewise, oxide growth during periods of process change – for example, temperature ramping or gas purging – has similar effects. If the oxidation time remains fixed, the result is an unpredictable deviation of oxide thickness from the value expected using oxide growth curves. With thinner oxides, the time during which steady-state conditions exist in the furnace is reduced and these transient effects become increasingly significant.

Control can be improved by careful assessment of the complete oxidation process. In the method presented here this is realised by simulation. An oxide growth simulation prog-ramme may be used to calculate the effect of interacting process parameters such as oxidising ambient and wafer temper-ature. A set of rules can be applied to determine these para-meters from measured furnace variables. If measurements are made during processing, a real-time estimate of the oxide thickness can be obtained. This can then be used to deter-mine the conditions for the remainder of the oxidation and to terminate the process under conditions which will give the required film thickness.

3. IMPLEMENTATION

Furnace data is readily available from most digital furnace systems. Figure 2 shows how measured variables are collected by a digital temperature controller (DTC) and digital process controller (DPC) then passed to a remote computer (Apricot PC) housing the simulation program. The simulation is based on an increment form of the Deal-Grove oxide growth model, with additions to allow simulation over a wider range of oxidations.

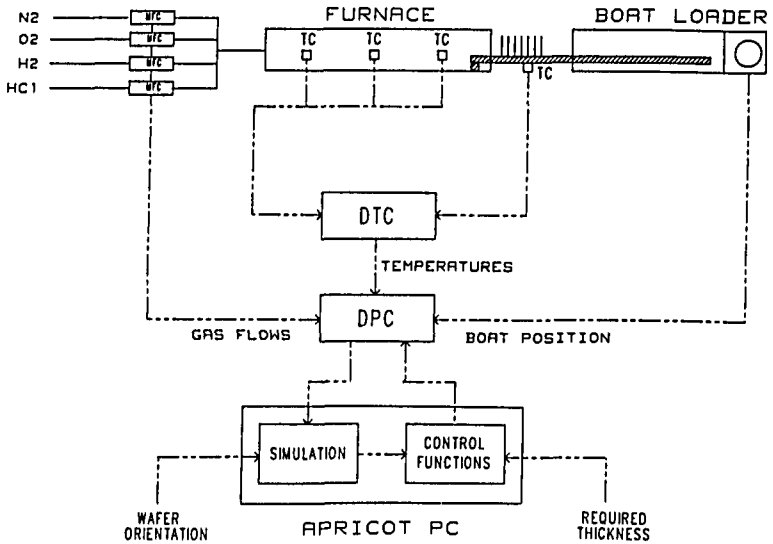$$\frac{\Delta x_o}{\Delta t} = \frac{B}{2x_o + A} + R$$

Figure 2
Data collection for computer simulation

where $R = C\ e^{(\frac{-x_o}{L})}$ models the rate enhancement observed for thin dry oxides.

The rate constants A and B are calculated from exponential expressions for the linear and parabolic constants.

$$K_L = {}^B\!/\!A = C_L\ e^{-E_{AL}/kT}.\ H_L.\gamma.P^n$$

$$K_P = B = C_P e^{-E_{AP}/kT}.\ H_P.P$$

where H_L and H_P are rate enhancement factors which model the variation in oxidation rate upon addition of HCl gas to the oxidising ambient. γ is a factor to model the oxidation rate for different crystal orientations of silicon. P is the partial pressure of oxidant.

The values of activation energy and pre-exponential constant depend primarily on the oxidising ambient. This is determined from flow rates of N_2, O_2, H_2 and HCl provided by mass-flow-controllers. P, H_L and H_P are also determined from gas flow data. A thermocouple positioned at the wafer-boat

provides data on wafer temperature, allowing the simulated oxidation rate to model more accurately that seen at the wafers.

During every 5 second time interval, current furnace data is passed to the computer to update the simulation. Rate constants are evaluated. The change in oxide thickness for that time increment is then determined. When the total oxide thickness approaches the required value, appropriate signals are sent back to the DPC to switch the furnace to an inert ambient and/or unload wafers from the furnace.

Since the whole oxidation process is continuously monitored, the system can automatically adjust for transient thermal effects and so enhance process accuracy and repeatability.

RESULTS

The feasibility of the simulation control procedure was examined by testing its ability to deliver a specified oxide thickness. Although any oxidation process would be suitable as a trial, one which involves substantial oxide growth under dynamic conditions gives a much more demanding test of the system capability. A convenient method of performing this is to incorporate a temperature ramp in an oxidising ambient into the furnace treatment. The furnace treatment used therefore consisted of the following sequence of steps:

1. Load wafers into furnace at 700°C in O_2.
    Step time = 10 min.

2. Ramp temperature to 950°C at 10°C/min in H_2O.
    Step time = 25 min.

3. Oxidise at 950°C in H_2O until the total oxide thicknness equals 1000Å (see below).

4. Anneal at 950°C in N_2. Step time = 10 min.

5. Unload wafers from furnace at 950°C in N_2.
    Step time = 5 min.

Determination of the oxidation time in step 3 requires estimation of the oxide grown during temperature ramping (step 2). This presents difficulty if a conventional furnace system is used, but the simulation control procedure will automatically and accurately take this oxide growth into account.

A recipe based on the above treatment was loaded into the DPC of a furnace configured for simulation control. This

recipe is needed to manage the individual furnace components: gas flows, temperature and boat loading. After being cleaned in boiling H_2O_2/H_2SO_4, followed by an HF dip then rinsing and drying, thirty <100> silicon wafers were placed in a quartz boat on the furnace boat loader. The simulation program was supplied with values for the required oxide thickness and wafer orientation then the furnace treatment was started. After the load and ramp steps, wet oxidation (step 3) cont-inued until the simulation had predicted the growth of 1000A. An instruction was then automatically sent from the Apricot-PC to the DPC to cease the oxidation and begin the anneal. After the anneal the wafers were unloaded from the furnace.

Four wafers equally spaced in the boat were selected for measurement. The oxide thickness on each was determined at five sites using a Nanospec. The mean thickness was 1008A with a variation of 2.2%.

Figure 3 show the temperature measured at the wafer boat during processing and figure 4 shows the corresponding oxide growth, computed real-time using temperature and gas flow data.
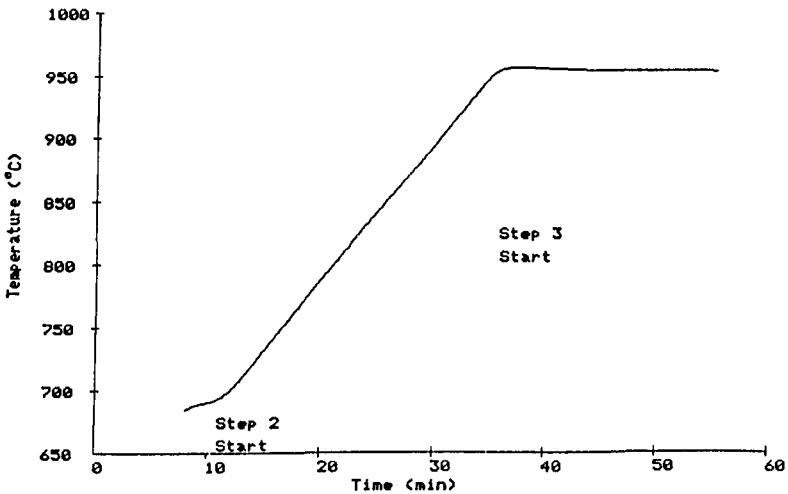

Figure 3
Temperature measured at wafers

At the end of the temperature ramp, it can be seen that an estimated 290A of oxide has grown. This is a significant proportion of the total oxide thickness, emphasising the need for careful assessment of oxide growth during temperature ramping. Oxidation has continued for a further 18 minutes
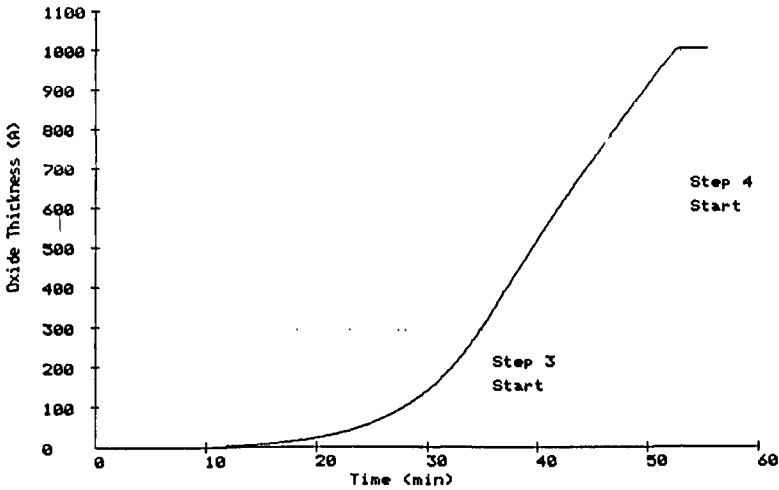
Figure 4
Simulated oxide growth

before the change to an inert ambient for annealing. This time has been proven correct, but it is based on furnace conditions during this particular run only and does not represent the 'standard' time required for step 3 of this process. Simulation control will always adjust this time as necessary to ensure growth of 1000Å oxide.

CONCLUSIONS

The agreement between desired oxide thickness and the value obtained after processing demonstrates the feasibility of simulation in a control application. The technique has accommodated dynamic process conditions in the form of a deliberately introduced temperature ramp. Other transient periods can similarly be assessed. This effective improvement in process control over conventional systems, which rely entirely on negative feedback loops, is an important factor in achieving the thickness tolerances required for VLSI.