A DEVICE SIMULATOR FOR SILICON ON INSULATOR MOSFETS

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ABSTRACT

A device simulator which predicts the dc characteristics of SOI MOSFETs has been developed. The simulator which is an extension of the MINIMOS program uses finite difference methods to solve the semiconductor equations in two dimensions for both carrier types. Accurate predictions of the onset of the "kink" effect have been made for a range of devices with different gate lengths, fabricated in SOI films formed by buried oxygen implantation. The influence of carrier mobility and interface charge at the lower interface on the subthreshold behaviour has been considered.

1. INTRODUCTION

There is currently much interest in the development of Silicon on Insulator (SOI) substrates for high performance VLSI circuits, particularly for CMOS devices [1, 2]. These substrates will allow fabrication of high density circuits with simplified processing, complete freedom from latch-up, and high speed operation, resulting from the reduced paristic capacitance to the substrates. One of the significant features of SOI MOSFETs is the floating island which gives rise to a "kink effect" in the I - V characteristics. This kink in the drain current occurs when majority carriers, generated by impact ionisation, flow into the neutral substrate and raise the electrical potential there [3]. This floating island effect can alter circuit performance because of transient overshoot in the drain current [4], and frequency dependence of propagation delay due to gate-island coupling [5]. It is therefore desirable to have a device

simulator capable of accurately predicting the onset of this effect and providing an indication of those physical parameters on which it is most dependent.

The two-dimensional device simulator MINIMOS [6,7] is widely used to simulate standard MOS devices, but in its most recent version 2.2, it does not have a capability to investigate the dc characteristics of an SOI MOSFET. In this paper we report an extended version of MINIMOS which models correctly the current flow mechanisms characteristic of floating island devices. The modified program takes full account of the revised boundary conditions at the interface between the silicon and the insulator.

2. *DEVICE EQUATIONS*

The fundamental model which describes the steady-state characteristics of an SOI MOSFET is governed by the three basic partial differential equations - Poisson's equation and the electron and hole continuity equations.

$$\nabla^2\psi = -q\frac{(p - n + N_D - N_A)}{\varepsilon} \quad (1)$$

$$\nabla.\underline{J}_n = -q(G - R) \quad (2)$$

$$\nabla.\underline{J}_p = q(G - R) \quad (3)$$

The electron and hole currents are described by

$$\underline{J}_n = -q(\mu_n n\nabla\psi - D_n\nabla n) \quad (4)$$

$$\underline{J}_p = -q(\mu_p p\nabla\psi + D_p\nabla p) \quad (5)$$

where the diffusivity D and carrier mobility μ are related by Einsteins relationship. The carrier mobility is strongly dependent on various scattering mechanisms giving rise to a highly non-linear dependence on electric field. The problems associated with the implementation of an appropriate mobility model for SOI MOSFETs are considered in more detail in section 5.

The generation term, G and the recombination term, R, in the continuity equations (2) and (3) are modelled by three processes; avalanche generation due to impact ionisation [8], Auger recombination due to direct band to band transitions [9], and thermal generation and recombination [10]. These mechanisms are well modelled by the following equations:

$$(G - R)_{avalanche} = \frac{|J_n|}{q} A_n \exp\left(\frac{- B_n |J_n|}{\underline{E} \cdot \underline{J}_n} \right) + \frac{|J_p|}{q} A_p \exp\left(\frac{-B_p |J_p|}{\underline{E} \cdot \underline{J}_p} \right) \tag{6}$$

$$(G - R)_{Auger} = (n_i^2 - np)(C_n n + C_p p) \tag{7}$$

$$(G - R)_{thermal} = \frac{n_i^2 - np}{\tau_n (p + n_i) + \tau_p (n + n_i)} \tag{8}$$

where τ_n and τ_p are lifetimes for electrons and holes respectively. A_p and and A_n are ionization rates for holes and electrons and B_p and B_n are exponential scaling factors which model the dependence of ionization rate on the magnitude of the electric field in the direction of current flow. C_p and C_n are Auger recombination parameters. The values for these parameters which are used in the simulation are summarised in Table 1.

Parameter	Value
τ_n, τ_p	10^{-8} sec
A_n, A_p	10^6 cm^{-1}
B_n, B_p	2.54×10^6 V cm^{-1}
C_n	2.8×10^{-31} cm^{6}sec^{-1}
C_p	1.0×10^{-31} cm^{6}sec^{-1}

TABLE 1 PHYSICAL CONSTANTS

Various authors have reported measurements of ionisation constants which can differ by more than an order of magnitude. We have found that the default values in MINIMOS are too low and tend to predict, for higher drain voltages, SOI drain currents greater than those measured experimentally. Consequently, we have used increased values of B_n and B_p to give a better fit to measured characteristics [15]. Similarly, the default values for carrier lifetime of 1 µsec have been found to be too high, and better results are obtained if the lifetime is assumed to be 10 ns or less. This seems a reasonable assumption since recombination in SOI devices occurs in the oxygen contaminated region close to the lower interface. Values of carrier lifetime have been shown

to affect the slope of the output characteristics for drain voltages greater than the "kink" voltage [3]. For smaller lifetimes, the "kink effect is less pronounced.

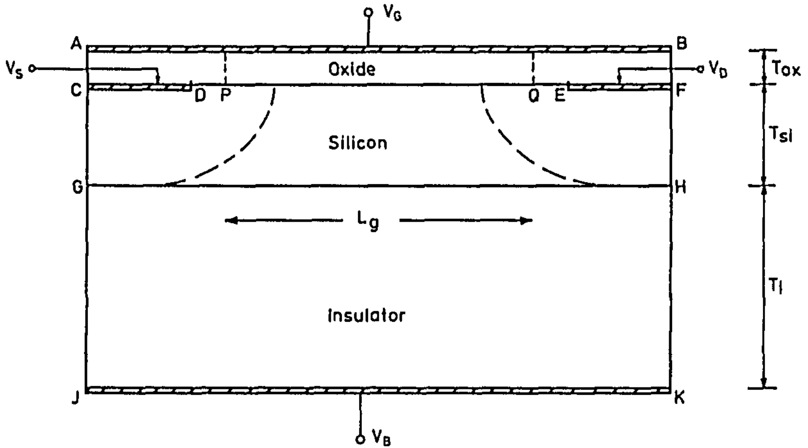


Fig.1 SOI MOSFET

3. *SIMULATION GEOMETRY*

The geometry of the simulated SOI MOSFET is shown in Fig. 1. At the source, drain, gate and insulator electrodes, electrostatic and Fermi potentials are derived from the applied voltages, while along the sides AJ and BK, Neumann boundary conditions are applied. At the gate oxide-silicon interface DE and the silicon-insulator interface GH, the equation

$$\nabla . \underline{D} = qN_{sc} \tag{9}$$

applies, where $\underline{D}$ represents the electric displacement vector and N_{sc} is the fixed surface charge density at the respective interfaces. In practice this positive charge is always accompanied by fast states distributed across the bandgap and located throughout the silicon, but principally located near the buried interface. No account of these fast states are included in the simulation.

The current continuity equations (2,3) are only solved within the silicon layer. It is assumed that there is no current flow into either the gate oxide or the insulator, i.e. the source current should always be equal to the drain current, unlike a conventional MOSFET where impact ionization can give rise to a significant bulk current. The extension of the gate contact over the source and drain contacts is an approximation to the actual device structure inherent in

MINIMOS. This approximation facilitates calculation of the coefficient matrices for the discretisation of the partial differential equations into a five banded system, using finite difference methods. The gate length defined from the mask is shown as the distance L_g. This distance is used to define source and drain diffusion windows. The source and drain contact CD and EF are normally separated from the source and drain diffusion windows by two mesh intervals in the x direction.

A number of changes have been made to the MINIMOS program. The mesh generator has been modified to ensure that a line of nodes defines the internal interface GH. The mesh grading in the y direction is arranged so that the minimum spacing of one hundredth of the silicon film thickness occurs at the oxide and insulator interfaces. The grading of the mesh in the silicon in both x and y directions is governed by criteria relating to the magnitudes of the doping gradient, carrier gradient, electric field and space charge, as defined in the original program. The iterative solver used for solution of Poisson's equation is unchanged except for modifications to the coefficients for those nodes lying along GH, and a zero space charge term for the insulator. The current continuity equations are solved within the reduced region CFHG using sparse matrix direct solution methods with minimum degree ordering of the coefficients [11]. This was found to be essential for the solution of the hole continuity equation, in order to obtain a balance of source and drain currents once sufficient impact ionization occurred to cause a "kink" in the characteristic. With the original iterative approach used in MINIMOS, it proved impossible to obtain overall convergence of the Gummel scheme for SOI devices, because the holes injected in the silicon layer by impact ionization cause a significant increase in the hole quasi-Fermi level within the source.

The input data format for the SOI simulator is identical to the original program, with an additional option which defines the film thickness, the insulator thickness, the density of fixed charge at the lower interface and parameter which defines the carrier mobility law as described in section 5. This amendment is easily incorporated by extending the existing command line interpreter so that it is capable of parsing the additional line of data.

4. *DEVICE TECHNOLOGY*

A number of approaches to SOI technology are being explored. One of the most promising is the synthesis of a buried oxide in a standard silicon wafer by the implantation of a massive does of oxygen [12]. Typically, for the devices reported in this paper, a dose of 1.8×10^{18} O^+

ions/cm^2 were implanted at 200 keV. Wafers are maintained at an elevated temperature of between 450 and 550°C during implantation to prevent the silicon surface being amorphised. The implanted oxygen forms a buried stoichiometric oxide of 0.5 microns underneath a surface layer, 0.25 to 0.3 microns thick, of silicon. The silicon layer is badly damaged and oxygen rich after implantation. Segregation of the oxygen to the interfaces and regrowth of the crystal structure is achieved by annealing at 1200°C for two hours. The resulting silicon layer can exhibit a reduced level of surface scattering with a mobility near the top surface of 80-90% of the bulk value [13]. The mobility profile through the depth of the film is a function of implantation temperature. For wafers implanted above 510°C, the silicon remains single crystal from the surface to the interface with the buried insulator. The increasing oxygen content and crystal damage with depth into the film result in a gradual reduction in mobility, with a value at the buried interface of 10-20% of the value at the top surface [14]. Implantation at temperatures below 500°C results in an oxygen rich polysilicon layer being formed between the surface single crystal region and the buried oxide. In this case the mobility at the buried interface is essentially zero.

The SOI substrates used in this study were implanted at the University of Surrey. Oxygen was implanted into the central regions of 3 inch (100) wafers. Beam heating was used to achieve the required implantation temperatures, resulting in a small radial temperature variation across the implanted zone [13].

5. MOBILITY MODEL

The default mobility model implemented in MINIMOS 2.2 is summarised in Table 2. The model is a combination of lattice scattering, impurity scattering, surface scattering and velocity saturation mechanisms as defined by the relevant equations. The surface scattering model is based on a phenomenological expression which is based on experience rather than rigorous theory. A full description of the theoretical basis of this model has been given [17].

There are several ways in which the mobility of n channel SOI MOSFETs differ from the default model. In order to model the very significant reduction of mobility with depth it was decided to allow the mobility at the lower interface to be input to the simulator as a defined parameter. This parameter was defined as a specific fraction of the bulk mobility. To match experimental observations [14], this value should lie in the range 0 to 0.2. A plot of the likely variation of mobility as a

Mobility Law	Equation	Electrons	Holes
Lattice Scattering	10	$\mu_o = 1430$ $\alpha = 2.3$	$\mu_o = 480$ $\alpha = 2.2$
Impurity Scattering	11	$\mu_{MIN} = 55.2$ $N_{REF} = 1.07\text{x}10^{17}$ $\gamma = 0.73$ $\beta = 3.7$	$\mu_{MIN} = 49.7$ $N_{REF} = 1.6\text{x}10^{17}$ $\gamma = 0.7$ $\beta = 3.9$
Surface Scattering	12	$y_{refo} = 5.0\text{x}10^{-7}$ $E_{cy} = 1.8\text{x}10^{5}$ $E_{cx} = 1.0\text{x}10^{4}$	$Y_{refo} = 4.0\text{x}10^{-7}$ $E_{cy} = 3.8\text{x}10^{5}$ $E_{cx} = 0.8\text{x}10^{4}$
Velocity Saturation	13	$v_{SAT} = 1.0\text{x}10^{7}$ $\beta_s = -0.87$	$v_{SAT} = 8.34\text{x}10^{6}$ $\beta_s = -0.52$
Total Mobility	14	$\beta' = 2.0$	$\beta' = 1.0$

$$\mu_L = \mu_o (T/300)^{-\alpha} \quad (10)$$

$$\mu_{LI} = \mu_L + \frac{\mu_L - \mu_{MIN}}{1+(N/N_{REF})^{\gamma}(T/300)^{-\beta}} \quad (11)$$

$$\mu_{LIS} = \frac{\mu_{LI}(y + y_{ref})}{y + y_{ref}(2 + E_y/E_{cy})} \quad (12)$$

$$y_{ref} = y_{refo}(1 + E_x/E_{cx})$$

$$\mu_{SAT} = (v_{SAT}/E_x)(T/300)^{-\beta_s} \quad (13)$$

$$\mu = (\mu_{SAT}^{-\beta'} + \mu_{LIS}^{-\beta'})^{-1/\beta'} \quad (14)$$

TABLE 2 MINIMOS 2.2 MOBILITY MODEL

function of depth is shown in Fig. 2. Over section AB of the characteristic the field dependence is calculated using the default model, with appropriate adjustment of the critical field for surface scattering. Over section BC, however, a quadratic fit with distance y, measured from the back interface, is employed, such that

$$\mu = \mu_T + (\mu_{MAX} - \mu_I)(y/y_{MAX})^2 \qquad (10)$$

where μ_{MAX} is the peak mobility as a function of depth, and μ_I is a variable data value expressed as a fraction μ_R of the low field bulk mobility, which is dependent on lattice and impurity scattering.

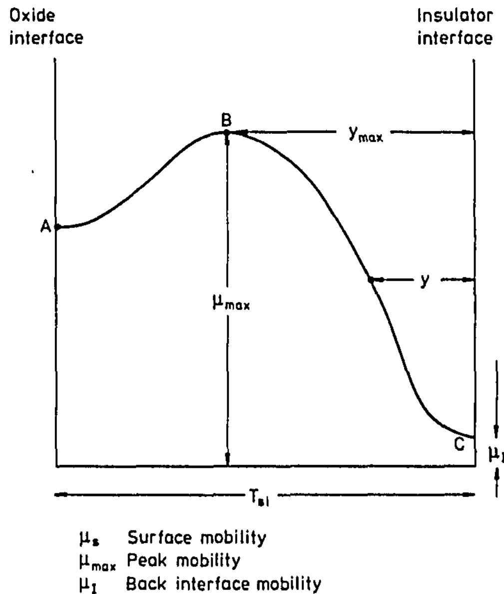


Fig 2 MOBILITY VARIATION WITH DEPTH

A second effect is a small increase in the electron mobility at the top interface due to lattice strain, produced by the interstitial oxygen [13]. This strain is known to increase the electron mobility along (100) surfaces by producing a shift in the conduction band minima [16]. To model this increased surface mobility, it was necessary to reduce the effect of the surface scattering mechanism by increasing the critical field for surface scattering by a factor of 5. This heuristic factor, the precise value of which is not absolutely critical, was determined by comparison of simulated and measured characteristics.

The final alteration to the default model involved reduction by a factor of 0.8 in the saturation velocity for electrons. There was no physical basis for this other than a better fit for short channel devices at high drain voltages.

6. *DEVICE SIMULATIONS*

SOI transistors were fabricated with a range of different gate lengths from 10 microns down to 1.5 microns and a constant gate width of 10 microns. The gate oxide thickness for all devices was 27 nm, the silicon layer thickness 0.3 micron and insulator thickness 0.5 micron. Source and drain regions were implanted with a dose of 5×10^{15} arsenic ions at 90 keV. All devices had two implants of boron through the gate oxide; 2×10^{12} ions/cm^2 at 100 keV and 6×10^{11} ions/cm^2 at 20 keV. The level of activation of the implanted boron in SOI is known to be less than the equivalent bulk case, possibly because of segregation of the boron to microprecipitates of silicon [18]. Also, some of the remaining oxygen present in the film will be electrically active, producing thermal donors. These two effects were taken into account in the simulation by halving the doping density resulting from the high energy implant. A plot of the resultant effective doping profile used in the simulations is shown in Fig. 3.

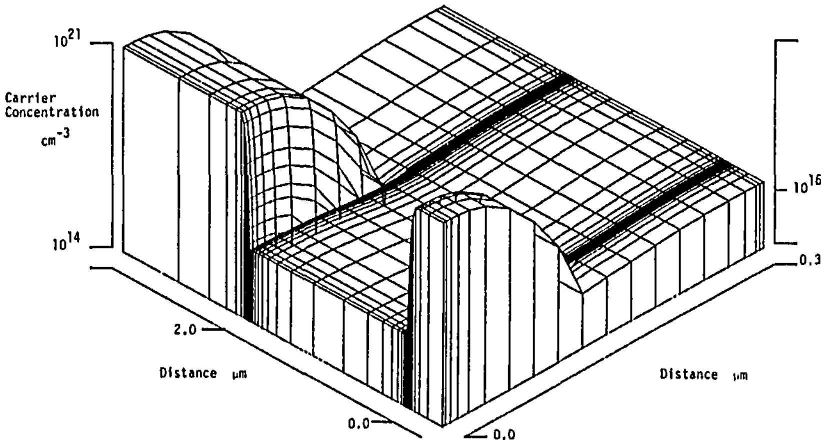


Fig. 3 DOPING PROFILE FOR 2 µm GATE LENGTH

The subthreshold characteristic of a 3 micron gate length device is shown in Fig. 4, for a drain voltage of 3 volts. This device was fabricated in a substrate at very low temperature implant, and exhibits negligible backchannel conduction. The threshold voltage, determined from the point at which the slope of the characteristic is a maximum, was found to be 0.8V. Excellent agreement with simulated results has been achieved for the subthreshold slope. For devices fabricated using implant temperatures greater than 510°C, the back channel of the transistor is turned on at zero volts substrate bias. This channel is caused by positive charges trapped at the buried interface. Negative substrate bias turns the back channel off, but its subthreshold slope is poor compared with the top channel, and a long tail is observed in the characteristic as shown in Fig. 5. These simulations, with a mobility ratio, μ_R of 0.05, indicate that the subthreshold conduction is very sensitive to the magnitude of the density of the interface charge. Although these results do not predict the shape of the subthreshold characteristic particularly well, they do give a very sensitive indication of the magnitude of the interface charge N_{sc}. The magnitude of this charge density is shown to be approximately 6×10^{11} cm^{-2} which is more than ten times the trapped charge density at the top oxide interface. A plot of the potential and electron charge density within the SOI device is shown in Fig. 6a and Fig. 6b respectively, for a gate voltage of 0.7 volts and a fixed charge density of 7×10^{11} cm^{-2}. This plot shows clearly both the formation of the conducting channel at the lower interface and the corresponding discontinuity in the electric field across this interface.

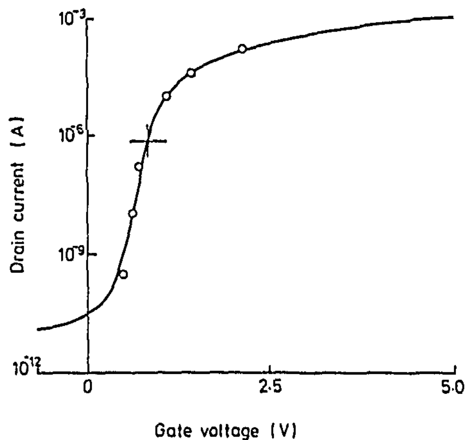


Fig. 4. THRESHOLD VOLTAGE CHARACTERISTIC FOR 3μm GATE

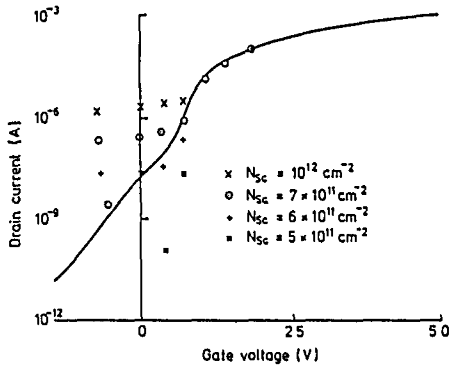


Fig. 5 EFFECT OF INTERFACE CHARGE ON SUBTHRESHOLD CHARACTERISTIC

(a) Electric Potential

(b) Electron Concentration

Fig. 6 CONDUCTING CHANNEL AT LOWER INTERFACE

The influence of the interface mobility on the subthreshold characteristic is summarised in Fig. 7, for two values of silicon layer thickness. Two measured characteristics are shown - one for a device with low subthreshold leakage and the other for a device with higher leakage in the dashed curve. This device corresponds to an implant temperature greater than 500°C, giving rise to a higher interface mobility and correspondingly higher leakage current. This is confirmed by simulation for two different values of mobility ratio, differing by two orders of magnitude.

Figs. 8, 9 and 10 show the dependence of the "kink" effect on the gate length. All these transistors come from the same chip. It can be seen that the simulator predicts the onset of the "kink" effect for a range of gate lengths down to 2 microns. The "kink" effect is less pronounced for shorter gate lengths. In these simulations the value of interface charge density has been assumed to be zero. This excellent agreement is very encouraging in view of the number of largely unknown parameters, such as mobility, lifetime and ionisation rate, which must be specified.

The distribution of both minority and majority carriers together with the corresponding generation/recombination rate, for a gate voltage of 3 volts, is shown in Fig. 11 and Fig. 12. At a drain voltage of 3 volts, the peak avalanche generation rate of 1.4 x 10^{23} cm^{-3} sec^{-1} at the edge of the drain diffusion close to the oxide interface, causes a small hole current to flow through the silicon film to the insulator interface, where the holes recombine with electrons injected at the source junction. The electron density in this region is 10^{11} cm^{-3} and the peak recombination rate is 10^{21} cm^{-3} sec^{-1}. A 1 volt increase in drain voltage, however, gives a peak generation rate of 6.0 x 10^{26} cm^{-3} sec^{-1}, an increased hole current and a correspondingly increased peak recombination rate of 6 x 10^{23} cm^{-3} sec^{-1} and electron density at the insulator interface of 2 x 10^{15} cm^{-3}. Indeed, within the source region, the Auger recombination term in the continuity equations becomes significant and can be more than an order of magnitude larger than recombination via trap levels. The electron and hole current densities for the latter case are shown plotted on a logarithmic scale in Fig. 13. Both hole and electron current densities have increased by more than 10 at the source junction adjacent to the insulator interface, for a 1 volt increase in drain voltage. Nevertheless in SOI devices the dominant current flow is still due to electrons even for drain voltages greater than the "kink" voltage. The magnitude of the hole current is still more than 10^4 smaller than the electron current which has its peak density at the surface.

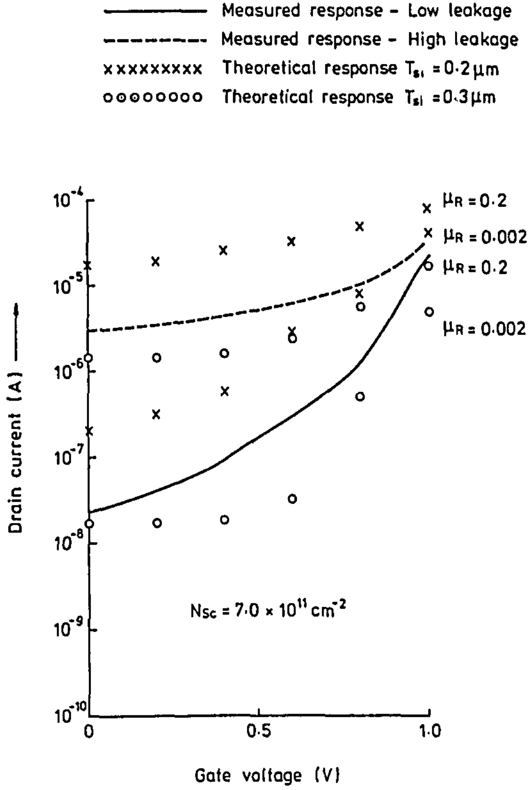


Fig.7 EFFECT OF MOBILITY RATIO μ_R ON SUBTHRESHOLD CHARACTERISTIC

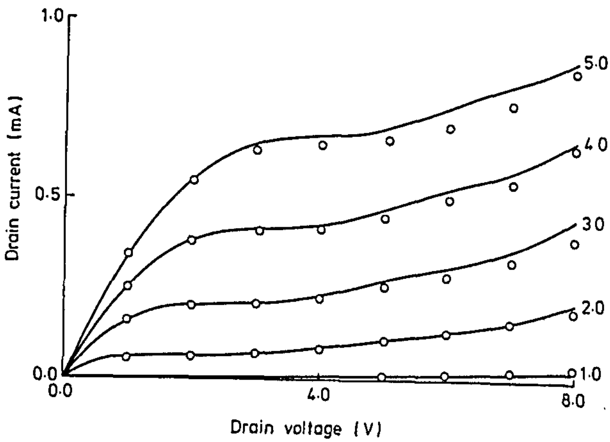


Fig. 8. OUTPUT CHARACTERISTICS FOR 5μm GATE

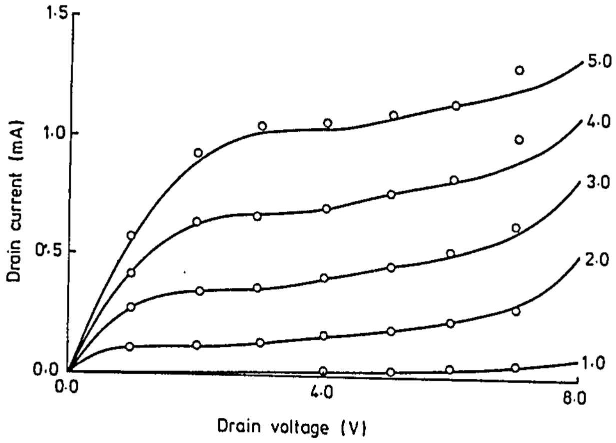


Fig. 9. OUTPUT CHARACTERISTICS FOR 3μm GATE

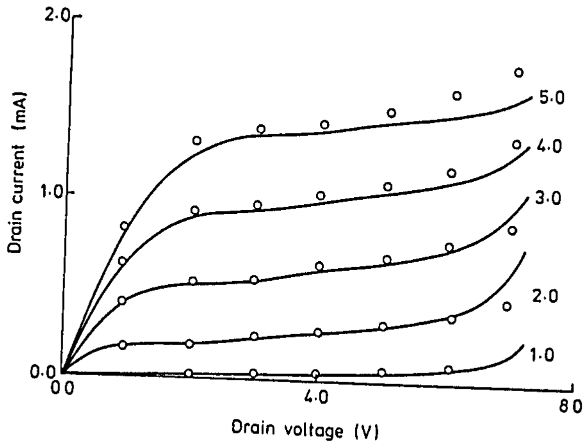
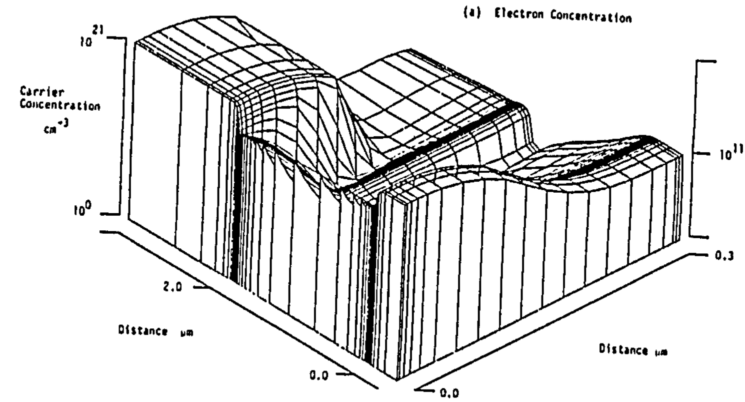
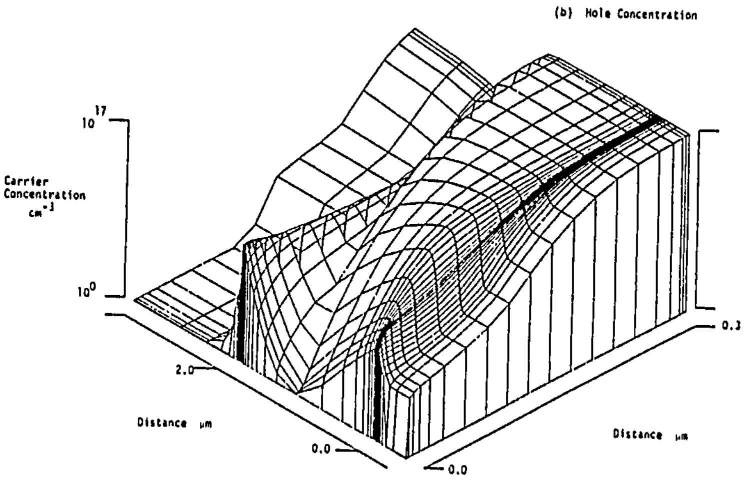


Fig. 10 OUTPUT CHARACTERISTICS FOR 2 μm GATE





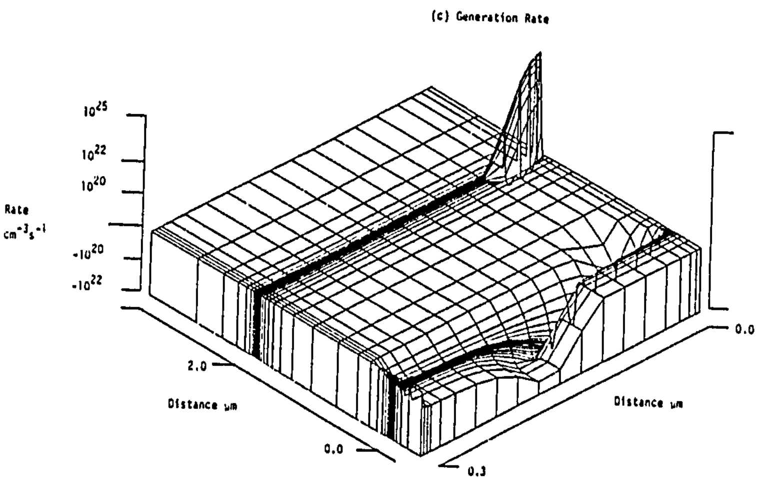


Fig 11 CARRIER DISTRIBUTION FOR V_{DS} = 3 VOLTS

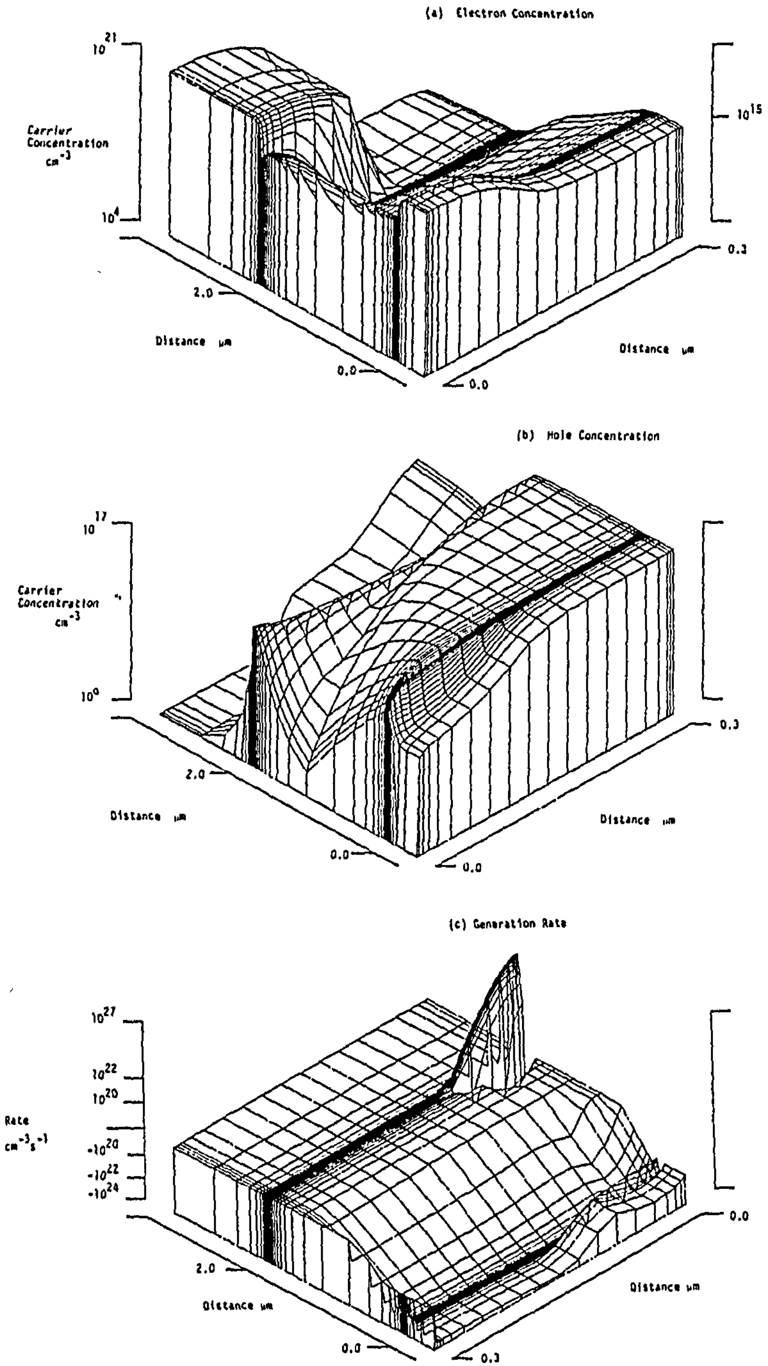
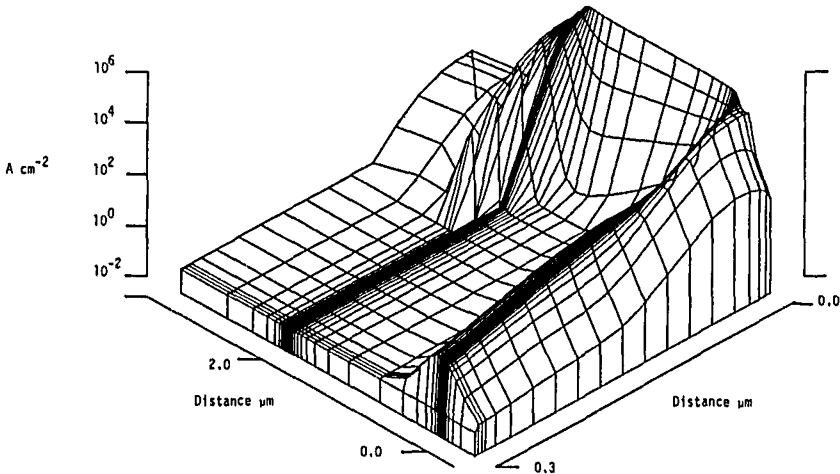


Fig 12 CARRIER DISTRIBUTIONS FOR V_{DS} = 4 VOLTS



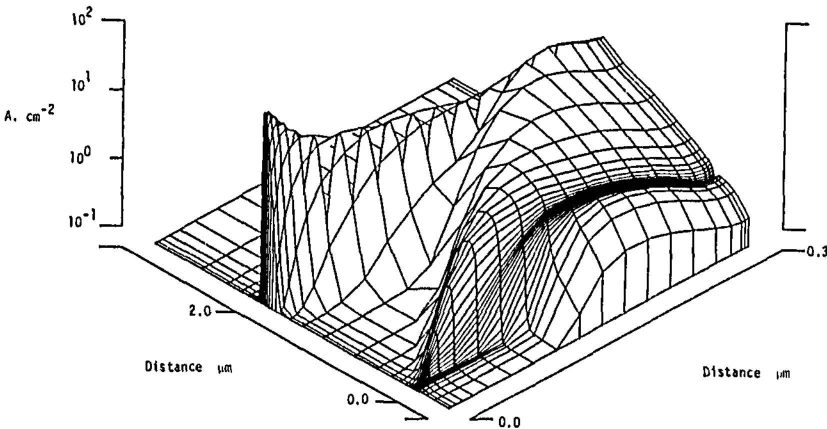


Fig. 13 CURRENT DENSITY DISTRIBUTION FOR V_{DS} = 4.0 VOLTS

7. *CONCLUSIONS*

Some initial simulations of n-channel SOI MOSFETs fabricated using oxygen implantation have been presented. Using a modified mobility model, excellent agreement with measurements has been achieved for a range of gate lengths down to 2 microns, for device operation above and below threshold. The subthreshold characteristic has been shown to be very sensitive to the magnitude of the fixed charge at the lower interface. Accurate predictions of the level of fixed charge at the lower interface can be made from the subthreshold slope in a low leakage device. Devices fabricated with higher temperature oxygen implants exhibit higher interface mobility and consequently higher subthreshold leakage.

ACKNOWLEDGEMENTS

The authors wish to acknowledge the assistance of S. Selberherr in making available the source code of MINIMOS 2.2 and also to S. Murray for summarising the MINIMOS mobility model. Dr P. Hemment and Mrs K. Reeson supplied the oxygen implanted wafers. This work is published with the permission of the Director of Research, British Telecom and was partially supported by a research grant from the Alvey Directorate.

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