Pre-Processor Geometry, Temperature and Parameter Modelling of Short and Narrow MOSFETS for VLSI Circuit Simulation, Optimisation and Statistics with SPICE *

G.T. Wright and H.M. Gaffur
Electronic and Electrical Engineering Department
University of Birmingham, Birmingham B15 2TT, England.

ABSTRACT

A parameter measurement and modelling method is described for the SPICE-2 level-3 MOSFET. Geometry dependences are modelled outside the simulator with simple polynomials which are incorporated into a pre-processor for parameter generation and circuit file construction. Operating point dependencies of threshold, body-effect and channel width are incorporated into an enhanced device model inside the simulator. The method is of general application and can be applied to any circuit simulator containing any transistor model.

1. INTRODUCTION

A major requirement for the construction and use of MOSFET models for CAD of VLSI is the provision of a sufficiently accurate but simple description of the geometry, temperature and operating point dependencies shown by many of the model parameters. A further requirement is that it should be possible to derive the model parameters themselves by straightforward measurements on a few, simple, test structures. The work to be described is based on the level-3 MOSFET model implemented in SPICE-2.[1] This is essentially the gradual-channel space-charge-limited approximation[2-6] and is a basic widely used representation.

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* This work has been described in part at the UK SPICE User Group Meetings held at Malmesbury, UK, in December 1982 and at Rutherford-Appleton Laboratory, UK, in March 1983, at the EEC Device Modelling Workshop held at Villard-de-Lans, France, in November 1983 and at the IEEE Device Modelling Workshop held at San Diego, USA, in February 1984.

Much work has been carried out and has been reported in the literature, in attempts to derive accurate, simple, closed, analytical expressions for parameter dependencies on geometry and temperature.[7-9] However, due to the essentially three-dimensional structure and complicated physical operating mechanisms of the short and narrow transistors used for VLSI circuits it is unlikely that this kind of approach will ever be successful. A practical engineering solution has been sought, therefore, by fitting simple polynomials in length and width to the parameter values obtained from measurements made at the operating temperature.

2. PARAMETER EXTRACTION

In order to use this method a satisfactory procedure for parameter extraction must be established. The interactions between parameter values are sufficient so that for any individual device there are many combinations of values which will provide a working fit to measured characteristics. It is not always clear, therefore, which are the "correct" values. If it is desired to describe device characteristics over wide ranges of length and width the procedure adopted must be capable of providing a smooth and systematic dependence of parameter values on geometry rather than the irregular variation so often obtained. It is desirable, as well, for the parameters and their values to be physically meaningful. These requirements can be satisfied by using a transistor model based on "good" physics and by a suitable sequence of measurements in which parameter values already obtained are "frozen" and used to evaluate further parameters.

The first and most basic parameters are those which determine the electrical lengths and widths of the transistors. These can be obtained from measurements of zero bias drain resistance against mask length and zero bias drain conductance against mask width.[10] MOS capacitor measurements give gate-oxide thickness and from all these results the surface-channel low-field mobility can be found. Typical sets of results for the measurement of electrical length and width are shown in Figs. 1 and 2. These were obtained on a matrix of self-aligned silicon-gate, n-channel transistors with lengths and widths on mask varying over the range from 2 to 50 micrometres. The length plots intersect as expected at the combined value of source plus drain series resistance. The width plots, however, intersect the horizontal axis at different places indicating a dependence of electrical width on gate bias. This is due to the fact that increasing gate bias inverts more of the silicon surface outward from the edges of the channel so increasing the effective channel width.

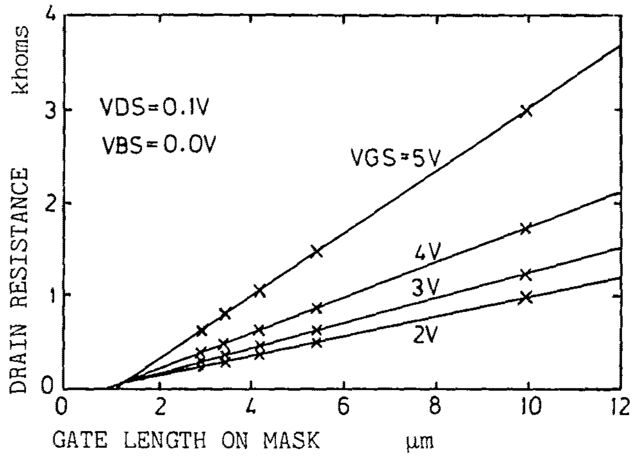

FIG.1 Drain Resistance Against Gate Length

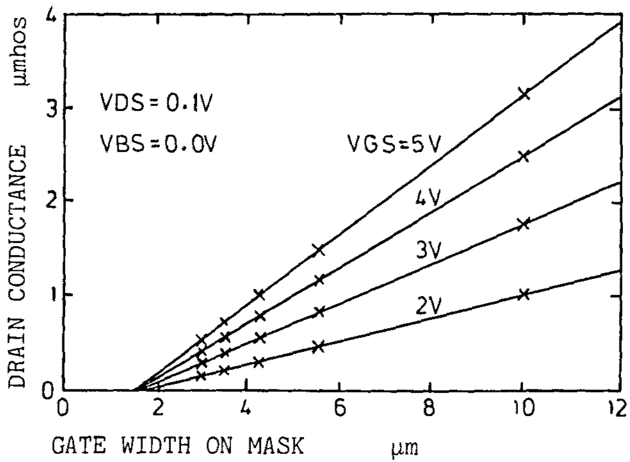

FIG.2 Drain Conductance Against Gate Width

A second group of parameters which can be measured directly and independently from gate turn on characteristics consists of the gate threshold voltage VTH, the coefficient γ for threshold dependence on substrate bias, the surface inversion potential ϕ, and the coefficient Θ for the gate field reduction of surface mobility. It is well-known that VTH and γ are functions of geometry because of electrostatic end and edge fringing effects which become significant at small dimensions. This is illustrated by Fig. 3 which shows the variation of gate threshold voltage with length and width for one set of transistors used in this work.

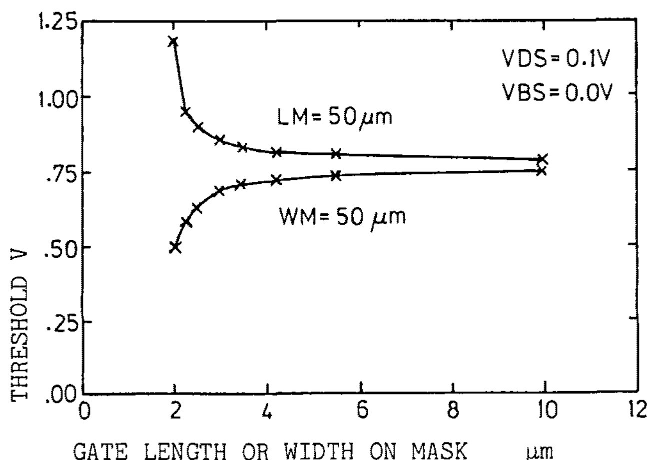

FIG.3 Variation of Threshold Voltage with Device Length or Width

However, the coefficient Θ as measured also shows a dependence on geometry. This is shown in Fig. 4 in which Θ is seen to rise as length falls and to fall as width falls. These variations are only apparent however; The dependence on length[11] due to the effects of source and drain series contact resistances and the dependence on width is a consequence of gate-field modulation of electrical channel width as described earlier. When these factors are taken into account the value of Θ becomes constant and independent of geometry. However, the value of Θ which is obtained in this way when the entire channel is virtually at source potential, is not the most suitable for use over the whole operating range. When the transistor has a significant drain voltage for example the average gate-oxide field is reduced and the effective value of Θ is reduced. The optimum, average, value of Θ over the full working ranges of gate, drain and substrate voltages is best

obtained in fact from the saturation characteristics of a long and wide device.

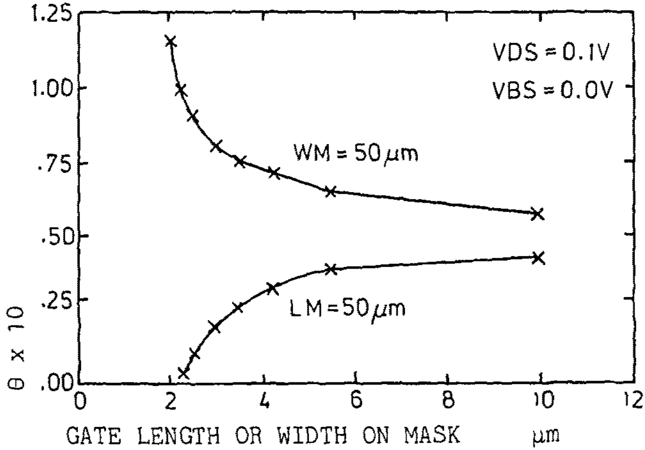

FIG.4 Variation of "Apparent" Θ with Gate Length or Width

Some designers use the apparent Θ as a means of including series resistance effects into the model. This is not a satisfactory procedure. The volts drop down the source resistance creates an effective dependence of gate threshold and of substrate bias upon drain current in all operating regions and the drain resistance reduces current in the triode region but has little effect in the saturation region. These effects become more noticeable and more significant as transistor dimensions become smaller. For satisfactory parameter evaluation procedures the measured characteristics of the transistor must first be corrected for source and drain resistance volts drop. If this is not done the remaining parameters, in order to compensate, show unnecessary and incorrect dependencies on geometry.

The most important remaining parameters of the level-3 model are VMAX describing drain field reduction of channel mobility, η describing drain-field modulation of the gate threshold and K describing the component of output conductance due to channel length modulation. These are intermingled in their influences upon the current-voltage characteristics of the transistor and are difficult to separate for direct measurements. The most satisfactory way to obtain them is to use least-squares curve-fitting of the full model equations to measured characteristics. With such a small number of parameters the values obtained are invariably consistent and unique.

The entire process of measurement and characterisation is carried out by an automated instrumentation system with analysis and evaluation handled by a linked, desk-top, computer system.

3. OPERATING POINT DEPENDENCE

Parameters such as gate threshold voltage, body-effect coefficient and electrical channel width vary in value as the operating point of the transistor changes. This is demonstrated by Fig. 5 which shows the dependence of gate threshold upon the square-root of substrate bias. Simple theory, based on uniform substrate doping, predicts a linear relationship between these quantities. This is not the case in practice and is a consequence of the markedly non-linear substrate doping under the surface channel caused by implantation. This is not allowed for in the level-3 model. The considerable variation of threshold shown for the narrow device is due largely to channel width modulation and this is not allowed for either.

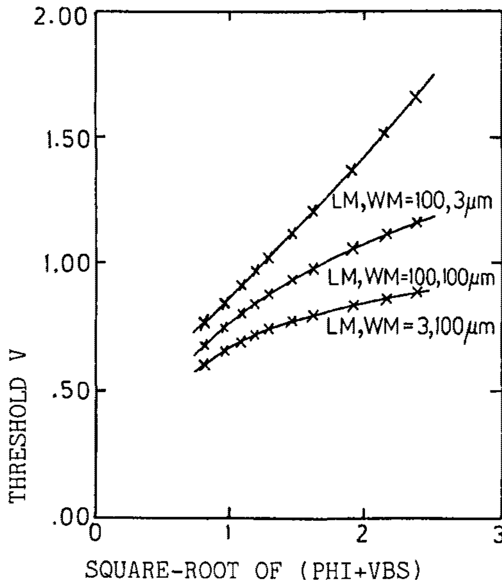

FIG.5 Threshold Voltage Against Square-Root of Substrate Bias

These mechanisms have been incorporated into the SPICE simulator by specification and use in the transistor model of three new parameters VTB, DWG and DWB. VTB is the threshold measured at a suitable substrate bias and together with VTH and γ enable the transistor model to use quadratic fits to the measurements shown in Fig. 5. In this way the threshold

voltage of the model can be made to follow closely that of the real device. Furthermore, the body-effect coefficient γ is now determined, as it should be, by surface doping at small substrate bias and by bulk doping at large substrate bias. DWG and DWB are the coefficients of channel width dependence upon gate and substrate biases respectively.

4. GEOMETRY DEPENDENCE

Gate threshold voltage and body-effect coefficient vary in value with both channel length and width whereas VMAX, η and K vary only with channel length. Circuit simulators such as SPICE incorporate algebraic relationships of various complexities to attempt to account for the relevant physical mechanisms. This approach has not proved particularly successful, creates unnecessarily intricate models and is computationally inefficient. The problems involved in generating accurate and general analytical models will worsen as device dimensions get smaller, as physical structures become more complex and as operating mechanisms get more complicated.

A practical working solution to the problem of geometry dependencies can be obtained by curve-fitting simple polynomials in length and width to the measured parameter values. Typical results of this procedure are given in Figs. 6 and 7 for threshold dependence on length and width. Simple theory suggests a reciprocal dependence for the change in threshold with change of dimensions consequently polynomials in 1/L and 1/W have been used. In each case a quadratic relationship has been found to give adequate accuracy of fit. The corresponding results for VMAX, η and K are given in Figs. 8, 9 and 10. These latter parameters are of significance only at small dimensions below about 4 micrometre; for larger devices the associated physical mechanisms become unimportant and the parameter values are irrelevant. The variation of VMAX with length is of interest in showing that this quantity is not physically meaningful in the SPICE level-3 model. This follows because it varies strongly with geometry instead of being constant and is a consequence of the fact that current saturation is defined in the model in terms of the low-field, rather than the high-field mobility. In most cases it has been found that linear or quadratic polynomials give sufficiently accurate results, particularly if these are combined with simple functional relationships suggested by elementary theory.

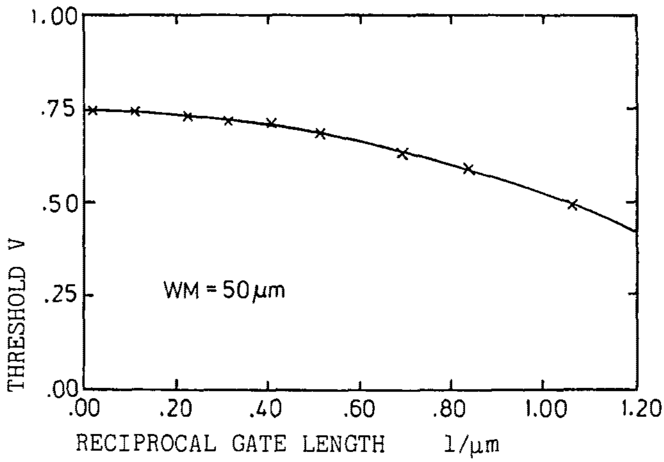

FIG.6 Threshold Voltage Against Reciprocal of Device Electrical Length.
Least-Squares Fit with Simple Quadratic

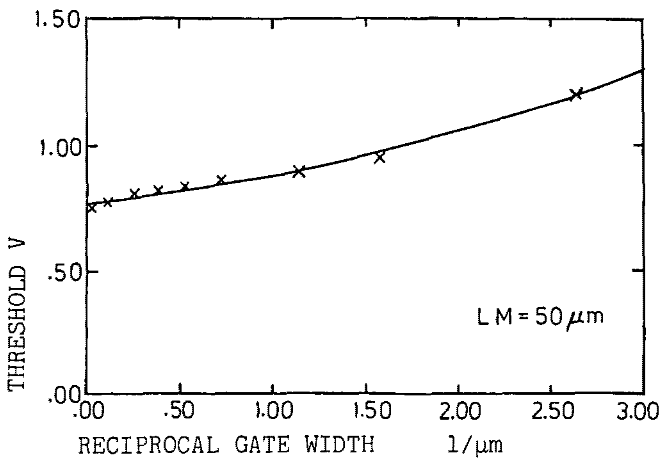

FIG.7 Threshold Voltage Against Reciprocal of Device Electrical Width.
Least-Squares Fit with Simple Quadratic

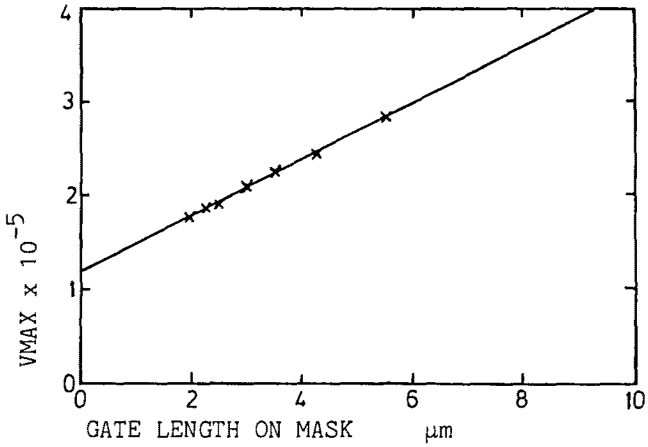

FIG.8 Variation of VMAX with Device Length for SPICE 2G.5 NMOS Level-3 Model. Least-Squares Fit with Straight Line.

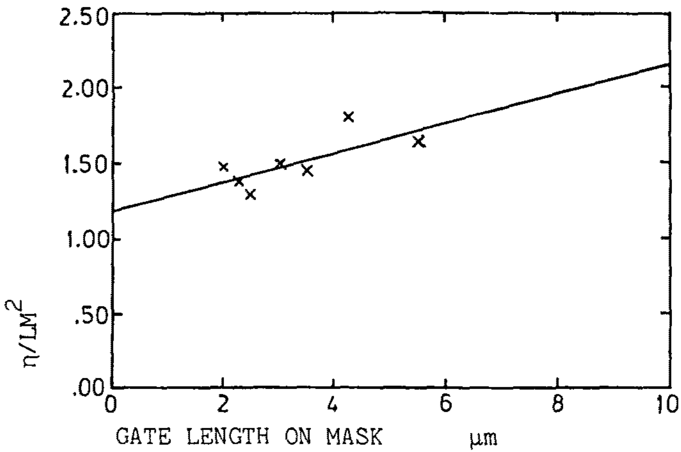

FIG. 9 Variation of η with Device Length for SPICE 2G.5 NMOS Level-3 Model. Least-Squares Fit with Straight Line.

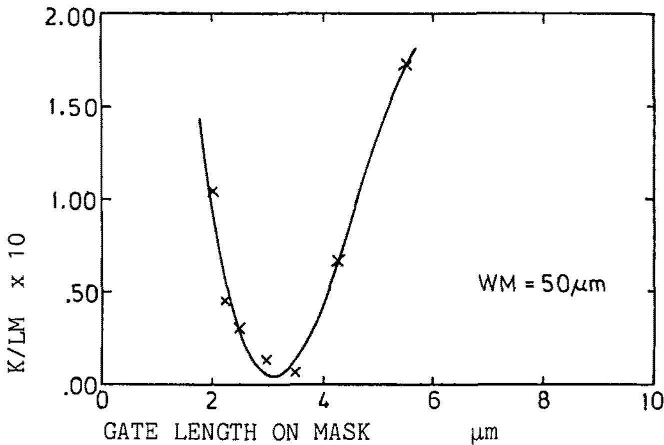

FIG. 10 Variation of K with Device Length for SPICE 2G.5 NMOS Level-3 Model. Least-Squares Fit with Cubic Polynomial.

5. PRE-PROCESSOR PARAMETER MODELLING

In order to use these results for circuit analysis and design it is necessary to make them available to the circuit simulator. If the circuit fabrication process has been established and is to be used for a considerable time then the simplest procedure is to insert the several polynomial equations into the model sub-routines of the simulator and omit the associated parameters from the circuit input file.

A more flexible and useful method is to incorporate the polynomial equations into a pre-processor which will generate the desired parameter values when required. This has been done as part of the present work. The pre-processor is constructed in FORTRAN and accepts as input any circuit file written in standard SPICE format. It reads the circuit file, calculates the entire parameter listings for each different transistor and then constructs the complete circuit file containing all parameter values for presentation to the SPICE simulator. By using these procedures a single set of parameter equations has provided a model fit of the order of 1% (average root-mean-square residual) over the range of transistor dimensions from 2 to 50 micrometres on mask in both length and width.

This methodology has several very useful advantages. First, for any given transistor model and for any given process the most accurate possible characterisation over the widest possible geometry range is obtained. The accuracy achievable is in fact considerably better than batch to batch consistency. However, any additional systematic variations due to modelling inaccuracies should always be reduced to a minimum. Second, by removing geometry dependencies from the simulator and placing them into the pre-processor the device model in the simulator is reduced to its simplest and computationally shortest form. Third, the circuit designer need not concern himself with model parameter values, calculations or listings. The circuit description file prepared by the circuit engineer requires specification of only length, width, area and periphery for each transistor; all parameter values are calculated and listings are constructed by the pre-processor which gives as its output the full circuit file for presentation to the SPICE simulator. Fourth, by measuring parameter values sequentially, physically meaningful "correct" values are obtained. This is important for reliable feedback to device designers and to process engineers. Finally, the principle outlined is completely general and can be applied to any simulator containing any model for any fabrication process.

The use of a pre-processor to carry out parameter modelling external to the circuit simulator itself improves the task of circuit analysis and design in several ways. For example, it is relatively easy and straightforward to examine the effects of parameter variations upon circuit performance. The desired changes are inserted once only into the pre-processor and this then implements the changes throughout the entire circuit description file. Further, the pre-processor and the simulator can be incorporated into an iterative loop to automatically adjust device dimensions and/or parameter values to converge on a desired circuit response or to optimise any desired aspect of circuit performance. Alternatively a cyclic loop can be used to step through a pre-determined sequence or to step through and examine the consequences of individual faults/or failures. The use of the pre-processor to examine yield statistics arising from process variations is shown in Fig. 11. This shows the statistics of propagation delay for an enhancement-depletion inverter stage caused by variations in channel length, channel width, oxide thickness and flat-band voltage. For purposes of demonstration these parameters have been assumed to have independent, normal, frequency distributions with quartiles in each case as shown on the diagram. In order to obtain these results the pre-processor and the SPICE simulator were incorporated into a cyclic loop together with routines to generate random numbers, to read and analyse the SPICE output and to store and plot the desired results. A full statistical analysis of this

kind is computationally lengthy of course particularly if a large circuit is being examined and might not often be justified. Nevertheless, the facility exists as and when needed.

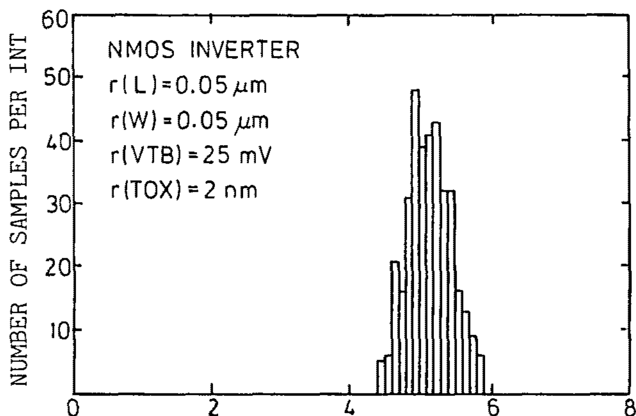

FIG. 11 Spread of Inverter Rise Times Due to Spreads of Parameter Values. Generated by SPICE 2G.5 with Statistical Parameter Pre-Processor.

6. CONCLUSIONS

A parameter measurement and extraction procedure has been described for the SPICE-2, level-3 MOSFET which provides accurate and reliable values. It has been shown that geometry dependencies can be modelled straightforwardly over wide ranges of length and width by simple polynomials. The use of a pre-processor to model parameter values outside the circuit simulator has been demonstrated. This enables the transistor model itself to be reduced to its simplest and computationally shortest form, eliminates the task of parameter listing for the circuit designer and provides a means for automatic circuit optimisation, reliability studies and yield statistics.

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8. REFERENCES

1. VLADIMIRESCU, A. and LIU, S.
"The Simulation of MOS Integrated Circuits"
Memo. UCB/ERL M80/7
Electronics Laboratory, University of California, U.S.A., 1980.

2. HOFSTEIN, S.R. and HEIMAN, F.P.
"Silicon Insulated-Gate Field-Effect Transistor"
Proc. IEEE, No. 51, p.1190, 1963.

3. WRIGHT, G.T.
"Space-Charge-Limited Surface-Channel Triode"
Solid-State Electronics, No.7, p.167, 1964.

4. IHANTOLA, H.K. and MOLL, J.M.
"Design Theory of Surface Field-Effect Transistor",
Solid-State Electronics, No. 7, p.423, 1964.

5. MERCKEL, G., BOREL, J. and CUPCEA, N.Z.
"An Accurate Large-Signal MOS Transistor Model for Use in Computer-Aided Design"
IEEE Trans. ED 19, p.681, 1972.

6. WRIGHT, G.T.
"Current-Voltage Characteristics, Channel Pinch-Off and Field-Dependence of Carrier Velocity in Silicon Insulated-Gate Field-Effect Transistors"
Elec. Lett., No. 6, p.107, 1970.

7. KLAASEN, F.M. and DE GROOT, W.C.J.
"Modelling of Scaled-Down MOS Transistors"
Solid-State Electronics, No. 23, p.237, 1979.

8. ENGL, W.L., DIRKS, H.K. and MEINERZHAGEN, B.
"Device Modelling"
Proc. IEEE, No. 71, p.10, 1983.

9. CHATTERJEE, P.K., YANG, P. and SHICHIJO, H.
"Modelling of Small MOS Devices"
IEE Proc. Pt. I, No. 130, p.105, 1983.

10. WRIGHT, G.T. and BANDALI, M.B.
"Experimental Study of Surface-Channel in Insulated-Gate Field-Effect Transistors"
Elect. Lett. No. 7, p.142, 1971.

11. CHATTERJEE, P.K., HUNTER, W.R., HOLLOWAY, T.C. and LIN, Y.T.
"Impact of Scaling Laws on Choice of n-Channel or p-Channel for MOS VLSI"
IEEE ED Lett., No. 1, p.20, 1980.