Non-planar Schottky Device Analysis and Applications

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Abstract

Nonplanar surfaces are becoming more important in device analysis. This is particularly true for Schottky-contact structures, which also present simulation difficulties in their own right. In this paper we present a new solution algorithm for simulation of Schottky structures, and study a device whose operation depends critically on the special properties of Schottky contacts.

Introduction

Schottky contacts have important applications in VLSI technology. Schottky-barrier p-channel MOSFETS (SB-PMOS) are attractive in CMOS due to their low minority carrier injection properties and their small junction depths[1]. Schottky barrier structures are also widely used in I^2L technologies[6-9].

The physics of Schottky junctions has been extensively investigated in the literature[2,3]. The majority carrier current flow in Schottky barriers is affected by several unusual phenomena including thermionic emission, tunneling, and barrier lowering. For example, when a Schottky junction is reverse-biased , as in the source contact of a SB P-MOS, the amount of current flow is primarily determined by two barrier lowering mechanisms, as discussed in [4,5]. These mechanisms are functions of the electric field across the junction, and therefore of the non-planar shape of the contact.

A model for 2D numerical simulation of non-planar devices including Schottky contacts must be simple enough not to burden an already time-consuming 2D simulation, but accurate enough to take into account these fundamental physical phenomena. We present here a new algorithm for simulating Schottky barriers , and we study a SB-PMOS which shows promise as a latchup-free CMOS device.

Numerical considerations

Two major differences in the treatment of Schottky contacts with respect to ohmic contacts arise. In the first place, a finite surface recombination rate is imposed at contacts. This introduces an equation for a new unknown, the carrier concentration, at each electrode node. This effect may be viewed as a special kind of current boundary condition. Secondly, the electrons experience an effective potential which is the sum of the internal Poisson solution and the external potential arising from image-force effects. Therefore the electron continuity equation is no longer solved consistently with the potential calculated from the Poisson equation, but rather with the effective potential, which is approximated by modifying the Poisson potential by the barrier lowering term.

The boundary conditions without barrier lowering are as follows:

$$\Psi_{S0} = \frac{E_G}{2q} - \Phi_{MS} \tag{1}$$

$$J_S = qS(n_S - n_{eq}) \tag{2}$$

where Ψ_{S0} is the surface potential, E_G the band gap, Φ_{MS} the work function difference between the metal and semiconductor, J_S the local current density at the surface, S the surface recombination velocity, and n_S and n_{eq} are the actual and equilibrium majority carrier concentration at the surface, respectively.

Following the thermionic emission theory, S can be expressed as

$$S = \frac{A^{**}T^2}{qN_m} \tag{3}$$

where N_m is the effective density of states in the conduction (valence) band for electrons (holes) as majority carriers and A^{**} is the effective Richardson constant that takes into account quantum mechanical reflection and tunneling. The electric field dependence of A^{**} has been investigated [4] and found to be small over the range of values encountered in practical cases. However small variations in the barrier due to barrier lowering are very important, because of its exponential influence on the current. Therefore a barrier lowering mechanism which accounts for both the image force and the dipole effect[4,5,6] is essential.

With barrier lowering, the effective surface potential can be expressed as:

$$\Psi_{Seff} = \Psi_{S0} - \beta \mathcal{E}^{1/2} - \alpha \mathcal{E} \qquad (4)$$

where β is the image force coefficient, α the dipole coefficient and $\mathcal{E}$ the electric field at the surface.

In order to satisfy the Poisson and continuity equation simultaneously, a variation on Gummel's method was implemented. Each Poisson solution is solved with boundary conditions

$$\Psi_S = \Psi_{S0}$$

then the majority carrier continuity equation is solved with

$$\Psi_S = \Psi_{Seff} \qquad \text{and} \qquad J_S = qS(n_{Seff} - n_{eqeff}) \qquad (5)$$

In (5) n_{Seff} and n_{eqeff} have the same meaning as in (2) but this time they have been computed using Ψ_{Seff} instead of Ψ_{S0}. The physical interpretation is that the Poisson equation is solved consistently with the charge, but that the electrons see a combined Poisson and image-force potential. This is in contrast to the more orthodox technique of solving the Poisson and continuity equations self-consistently, then changing the barrier height according to the field calculated and effectively solving with a new work function. The new method is 3-4 times faster than the latter, and in fact is as fast as solving standard ohmic contact structures. Moreover, the physical phenomena are well represented because the final barrier lowering is computed from the actual electric field present when convergence is reached.

Simulation Results

Fig.2 represents a cross section of a SB P-MOS showing the non-planar S/D electrode and the sidewall spacer between S/D and gate. The Schottky barrier P-MOS device[1] has been proposed to decrease the current-gain product of the two parasitic bipolar transistors responsible for latchup. Unfortunately the SB P-MOS transistor has very poor transconductance, one of the causes of which is the presence of the spacer between source/drain electrodes and the active channel, which prevents shorting between S/D and gate

due to silicide formation. A number of SB P-MOS structures with different geometries have been simulated to investigate the role of both Schottky contact and spacer with respect to transconductance degradation. The values of drain current for spacer widths varying from 0 to 1500 Å are shown in fig.3. Figure 4 illustrates the effective barrier lowering found at the edge of the contact for different structures, representing the different coupling between gate and source. Furthermore, figure 5 shows a comparison between a pure SB P-MOS and two lightly P-doped S/D Schottky P-MOS with, respectively, 3.10^{13} and $3.10^{14} cm^{-2}$ implant dose. Figure 6 shows the surface potential of the pure SB P-MOS and one of those with lightly P-doped S/D : the Schottky current emission mechanism due to barrier lowering produces a considerable voltage drop across the junction, adversely affecting the device performance ; however the voltage drop practically disappears in the presence of a lightly doped region. The conclusion to be drawn is that the presence of lateral doping at the source edge is far more important than the exact spacer dimensions in determining the portion of the drain voltage dropped across the source-channel junction. As a result, transconductance is a weak function of spacer size, but a strong function of lateral doping.

Conclusions.

A Schottky contact model suitable for application in 2D device simulations has been implemented. A non-planar Schottky structure, SB P-MOS for CMOS isolation applications, has been studied. The performed simulations show, in particular, the rule of the spacer for the structure.

References

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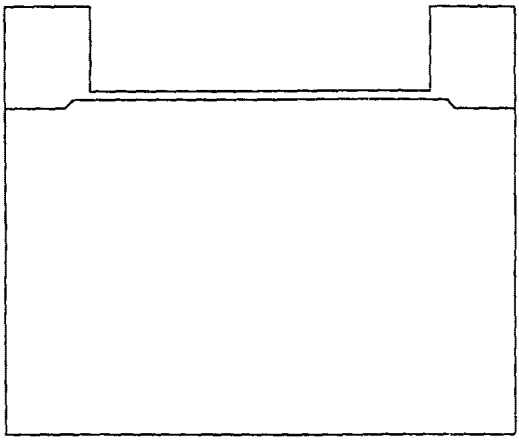

Fig. 1a Structure for simulation.

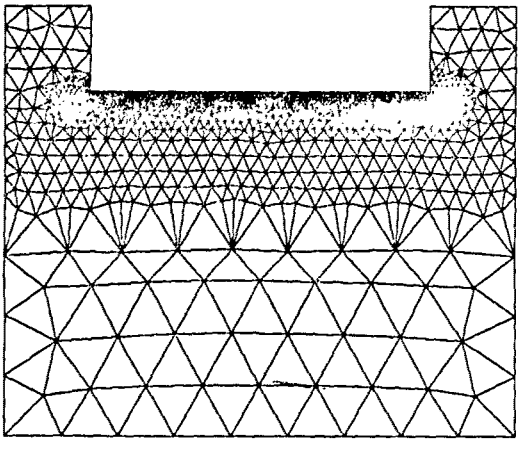

Fig. 1b Simulation grid.

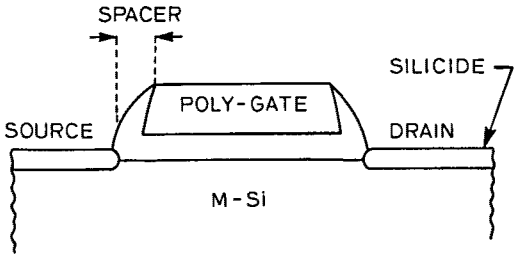

Fig.2 Schottky Barrier P-MOS

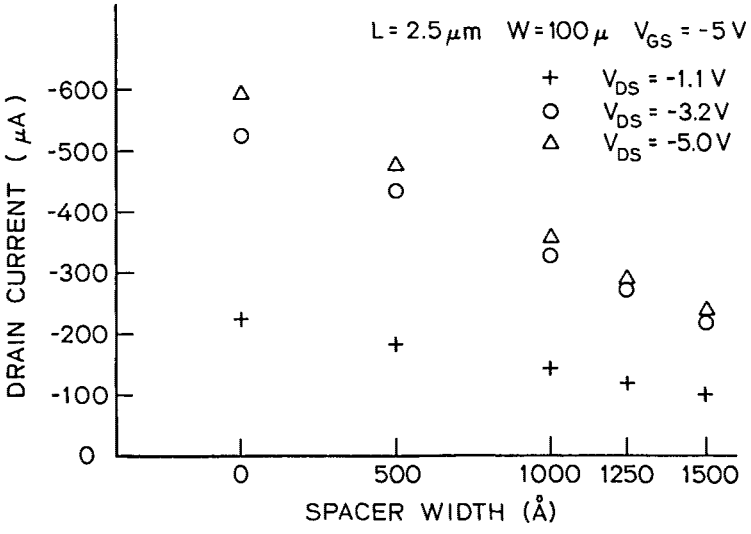

Fig.3 Drain current as a function of spacer width

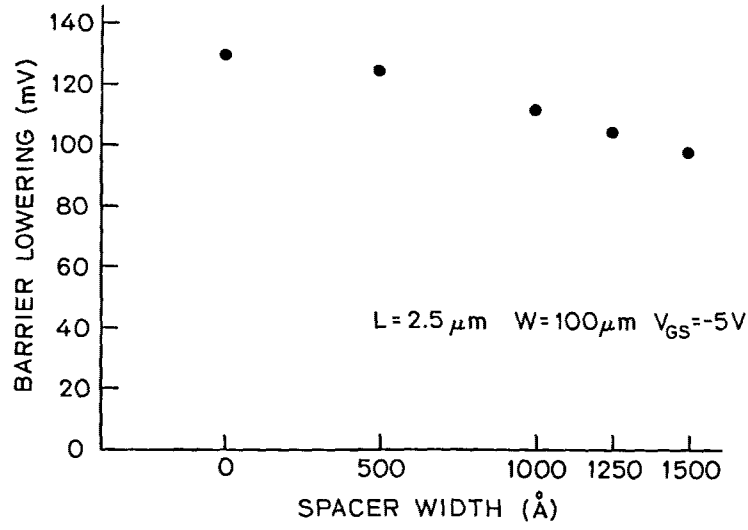

Fig. 4 Effective barrier lowering at the source edge as a function of spacer width.

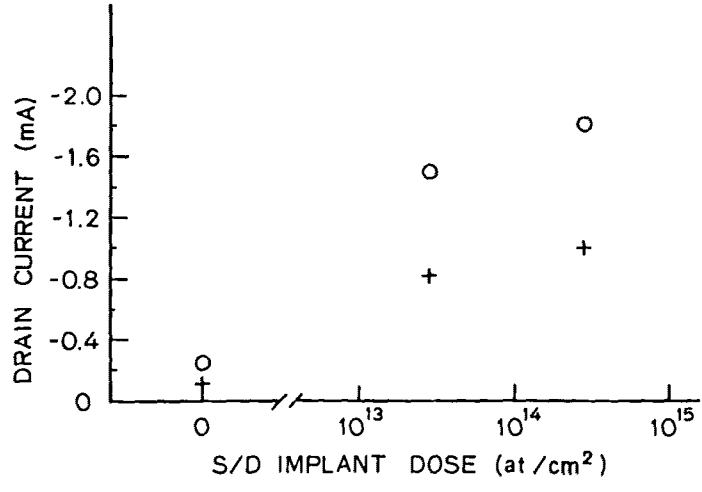

Fig.5 Drain current as a function of S/D dose for SB P-MOS

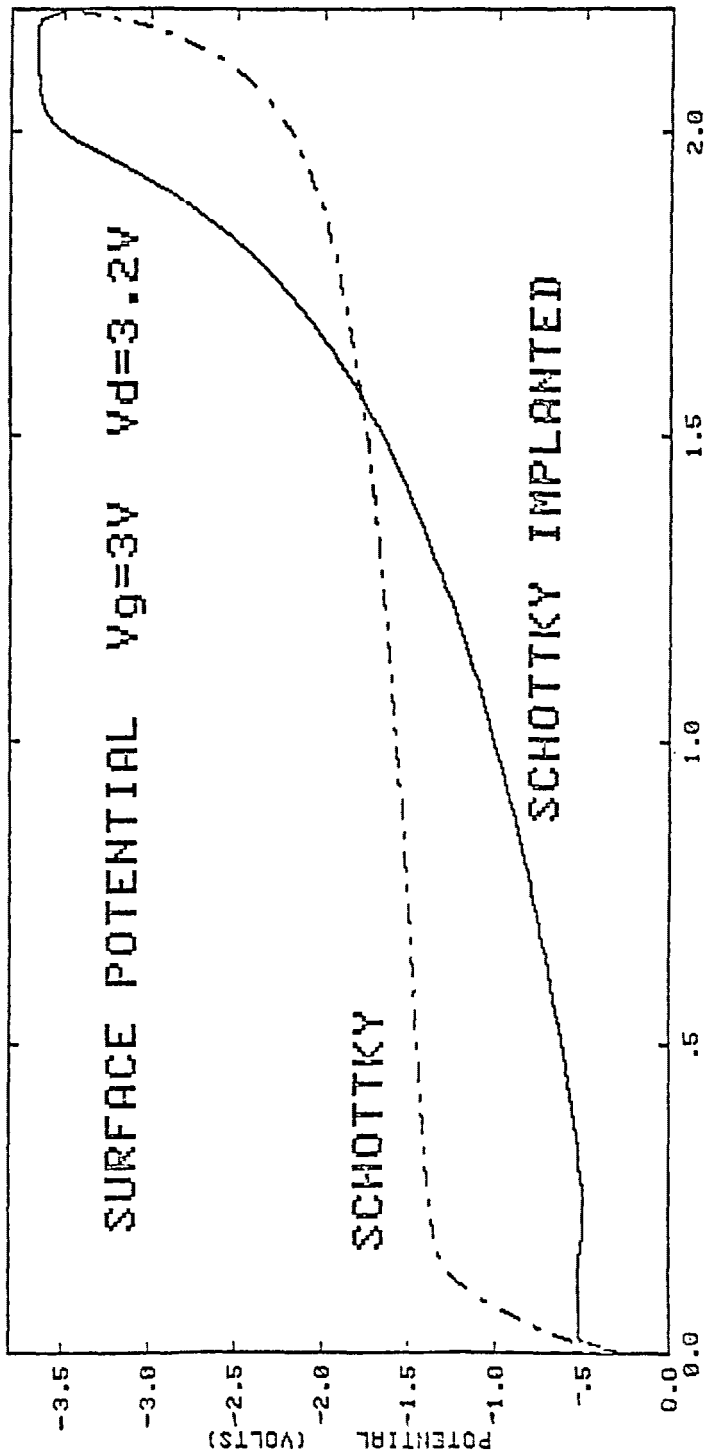

Fig.6 Surface potential of pure and lightly doped SB P-MOS