

TWO DIMENSIONAL NUMERICAL ANALYSIS FOR DEVICES
WITH FREE STEP DESIGN METHOD

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ABSTRACT

The algorithms for device simulation for arbitrary device structure and general analysis were studied, and a two dimensional device simulation program was developed. The program is composed of a pre-processor which functions as the user interface, and a device simulator that is independent of device structure. The pre-processor translates device structure data into the input data for device simulator. The pre-processor also determines the sequence of steps according to device type and purpose of analysis. In each step, solved equations, physical models, and convergence conditions are specified. Device simulation yields a numerical solution according to designed steps and gives a more accurate solution while using less computation time. The depletion layer analysis sets the initial condition for numerical solution independent of the device structure and bias conditions. The avalanche effect of n-channel MOSFETs was analyzed by this program. MOSFETs with four gates and npn-bipolar transistors can be analyzed only if user input data is changed. Programs having these algorithms can effectively analyze the arbitrary device structures with any bias condition, and can satisfy any user requirements.

1. INTRODUCTION

Two dimensional device simulation is useful for device design of MOS integrated circuits because the experimental investigation of device characteristics is time consuming. According to recent advances in IC process technology, the optimal design of MOS devices has been made more difficult because of their complicated structures, for example, LDD MOSFETs. Therefore device simulation programs are necessary to analyze complicated device structures.

Many programs [1][2][3] developed for MOSFET solve Poisson's equation and one current continuity equation for electron or hole. These programs require little computation time for analysis, but they omit the physical models such as carrier generation and recombination because the models are negligible in the long channel MOS devices under the normal bias condition. Several simulation programs [4][5][6] solve electrostatic potential, electron concentration, and hole concentration, and these programs analyze the avalanche breakdown phenomena in MOS devices. These above mentioned programs are still used exclusively for standard device structure. Some of these programs consume much computation time to analyze the device under higher bias conditions because they use thermal equilibrium as the initial condition for the numerical solution.

This paper focuses the algorithms for device simulation programs which analyze arbitrary device structures under any bias conditions. The algorithms also analyze standard devices using computation time comparable to that of the exclusive programs. To evaluate the algorithms for the program the Universal Semiconductor Analysis System (UNISAS) was developed. In section 2, an overview of UNISAS is introduced. UNISAS is composed mainly of a pre-processor and a two dimensional device simulator with free step design method. In section 3, the algorithm of the pre-processor is discussed. In section 4, the numerical and physical models used in the device simulator are explained, and a new method of setting the initial condition for numerical solution is discussed. In section 5, the simulation results and effectiveness of the program are shown and discussed.

2. OVERVIEW OF UNISAS

Conventional simulation programs can solve only standard device structures. But device designers need to analyze arbitrary device structure under any bias condition. These requirements increase the complexity of the algorithm and computation time of device simulation. The methods defining of device configuration and setting the initial condition for numerical solutions become more complicated due to dependence on device structure.

To solve these problems, a device simulation program and a new method of setting initial conditions are proposed. The program is composed of a pre-processor (PPDS) for user interaction, and a main processor (DSS) independent of the device structure. PPDS translates the input data of device configuration into detail information for numerical solution under DSS. The initial condition for numerical solution is set by depletion layer analysis, independent of the device structure for any bias condition.

In DSS the solved equations and physical models are prepared sufficiently for analysis of any device type, and these assortments may increase computation time. We proposed a new method, called the free step design method, to execute device simulation using equations and physical models suitable for analysis. This method keeps DSS independent of device structure. DSS is executed according to the step sequence, which include solved equations, physical models and convergence conditions for numerical solutions. DSS yields better solution with less computation time under this method. Under the free step design method, PPDS find the optimal steps considering device type and purpose of analysis specified by the user.

DSS is completely independent of device structure, or purpose of analysis.

Figure 1 shows a composition of UNISAS which includes PPDS, DSS, an one dimensional process simulator (ASPREM), and graphic output program (VDIOS). Input data from users is also shown in this figure. The impurity distribution is calculated by ASPREM, which is the improved SUPREMI[7] for multi-layer structures consisting of silicon-oxide, silicon-nitride and poly-silicon layers. Physical models, such as oxidation-enhanced diffusion are also improved. The results of the process and device simulations are sent to VDIOS and dispicted on graphic display. VDIOS can dispict contour-plots, birds-eye-views and so on. The circuit simulator receives the parameters of the device model calculated by DSS.

3. ALGORITHM OF PPDS

PPDS translates input data of device structures and finds the optimal step design of device simulation.

To translate device-structure data given by the user into input data for DSS, PPDS defines nodes and boundaries for numerical solutions. Nodes are the intersections of grid lines divided according to input data and position of pn-junctions. Boundaries on the device-configuration edge comprise a closed loop. Each node is classified by type of material such as semiconductor or insulator, and by its position in the grid space for numerical solution, for example, in, on, or outside the closed loop. The impurity distribution is mapped on each node according to input data. Boundaries that are chains of node are classified by numerical solution, for example, they are classified as having hold or free boundaries. DSS can perform device simulation if it reads the data with respect to the nodes and boundaries made by PPDS.

PPDS will specify the optimal sequence of steps for device simulation according to device type and purpose of analysis. For standard MOSFET devices one-carrier analysis is performed, then two-carrier analysis having an avlanche effect

is performed in order to decrease computation time. For device analysis of potential distribution with low current, one-carrier analysis with a higher accuracy of potential is used.

Input data from users is interpreted by language developed for this program. Users can define the device structures, the interfaces for ASPREM, the mapping method for two dimensional impurity distribution, physical models, convergence conditions for numerical solution, bias conditions, and the interface of VDIOS. For arbitrary device structures, users must describe detail information, for example, definition of geometrical elements which compose device configuration and definition of boundaries. For standard device structures like MOSFETs, input data for device structure is saved in a disk file, and the users can describe the input data to be changed.

Figure 2 shows an example of formats for one set bias analysis of n-channel MOSFET. These formats are simple and clear for user. Figure 3 shows the device geometry, the pn-junctions, and nodes for numerical solutions where PPDS has translated the input data of the n-channel MOSFET in Fig. 2. The grid intervals are smallest at the pn-junctions in the horizontal direction, and at the interface in the vertical direction, respectively, where the current densities change greatly.

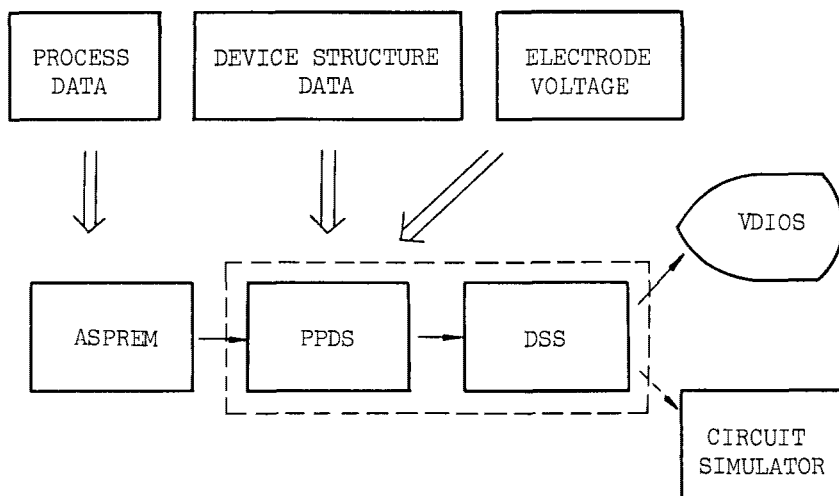


Fig. 1 Composition of UNISAS

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*ODESA
  DEVICE = MOSFET, SUBSTRATE = P
*DATA
  GATE.LENGTH = 2.0, GATE.THICKNESS = 0.03
  LFT.ELE = IMP, MOB.ELE = YAMAGUCHI
  GNR.ELE = IMPACT
  LFT.HOL = IMP, MOB.HOL = YAMAGUCHI
  GNR.HOL = IMPACT
*RUN
  VGS = 4.0, VDS = 7.5, VBS = 0.0
  OP.A.POT = MD
*END

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Fig. 2 Input formats of PPDS for standard n-channel MOSFET

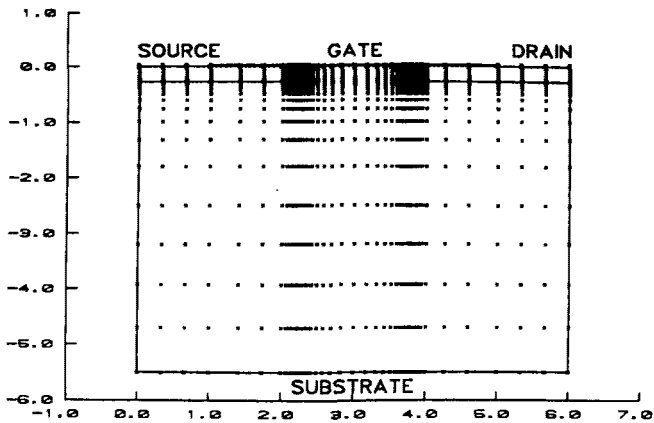


Fig. 3 Device geometry and discretization nodes for standard n-channel MOSFET

4. PHYSICAL AND NUMERICAL MODELS IN DSS

DSS performs device simulation independent of device structures and user requirements, according to the designed steps and the informations about nodes and boundaries. To set the initial condition for the numerical solution, depletion layer analysis is used because it is independent of device structure and bias condition.

4.1 Numerical models

In each step of device simulation, Poisson's equation and current continuity equation for electron and hole can be solved. The continuous forms of these equations in semiconductor are

$$\nabla(\epsilon\nabla\psi) = -q(p-n+\Gamma) - Q_{ss} \quad (1)$$

$$-\nabla \cdot J_n = G - R - R_s \quad (2)$$

$$\nabla \cdot J_p = G - R - R_s \quad (3)$$

where

$$J_n = -\mu_n n \nabla \psi + D_n \nabla n \quad (4)$$

$$J_p = -\mu_p p \nabla \psi - D_p \nabla p \quad (5)$$

Here, ψ , Γ , and Q_{ss} are electrostatic potential, impurity concentration, and charge concentration representing the fixed charge at the interface. n and p are the electron and hole concentrations, J_n and J_p are the electron and hole current densities, G and R are the generation and recombination rates, μ_n and μ_p are the electron and hole mobility, D_n and D_p are the electron and hole diffusivities, and ϵ and q are permittivity and the absolute magnitude of the electron charge. R_s is the generation-recombination rate at the interface. In Eqs. (2) - (5), J_n and J_p are normalized by q . In insulator n , p , and Γ is zero.

In DSS Poisson's equation (1) is linearized by Gummel's algorithm [8], and expressed as

$$\nabla(\epsilon \nabla \delta) - \frac{q^2}{kT}(p+n)\delta = -\nabla(\epsilon \nabla \psi^i) - q(p-n+\Gamma) - Q_{ss} \quad (6)$$

where $\delta = \psi^{i+1} - \psi^i$

Here, k , T , and i are Boltzmann constant, temperature, and iteration number, respectively. Equations (2), (3) and (6) are discretized on the rectangular grids. Figure 4 shows a rectangular cell with eight triangular subregions. A cell is the area inside the perpendicular bisectors of the lines joining the center node to the four nearest nodes. The lines joining the center node to the eight nearest nodes divide the cell into the eight triangular subregions. The finite difference equations at the center node can be derived by integrating Eqs. (2), (3), and (6) over the cell, using Green's theorem. The equations are shown as follows:

$$\begin{aligned} & \sum_{i=1}^4 \sum_{j=1}^4 (\epsilon_{ij} \frac{\delta_{ij} - \delta_0}{h_i} s_{ij}) - \frac{q^2}{kT}(p+n)S\delta \\ & = -\sum_{i=1}^4 \sum_{j=1}^4 (\epsilon_{ij} \frac{\psi_{ij} - \psi_0}{h_i} s_{ij}) - q(p-n+\Gamma)S - Q_{ss}l \end{aligned} \quad (7)$$

$$\sum_{i=1}^4 \sum_{j=1}^4 (J_{ni} s_{ij}) = -(G-R)S + R_s l \quad (8)$$

$$\sum_{i=1}^4 \sum_{j=1}^4 (J_{pi} s_{ij}) = (G-R)S - R_s l \quad (9)$$

where s_{ij} and ϵ_{ij} is the base length and the permittivity of the triangular subregion, and h_i is the distance from the center node to the nearest node. S and l is the area of semiconductor, and the length of the interface in a rectangular cell. If the interface does not cross the cell, l is equal to zero.

J_{pi} and J_{ni} are derived from Eqs. (4) and (5), using the technique of Scharfetter-Gummel[9]. J_{pi} and J_{ni} are

$$J_{ni} = \frac{\mu_{ni}(\Psi_0 - \Psi_1)}{h_1} \left[\frac{n_0}{1 - \exp(\Theta_n(\Psi_0 - \Psi_1))} + \frac{n_1}{1 - \exp(-\Theta_n(\Psi_0 - \Psi_1))} \right] \quad (10)$$

$$J_{pi} = \frac{\mu_{pi}(\Psi_0 - \Psi_1)}{h_1} \left[\frac{p_0}{1 - \exp(-\Theta_p(\Psi_0 - \Psi_1))} + \frac{p_1}{1 - \exp(\Theta_p(\Psi_0 - \Psi_1))} \right] \quad (11)$$

where Θ_n and Θ_p are the Einstein relations for degenerate carrier concentrations, and equal to q/kT under low carrier concentration. When bandgap narrowing effect is considered, the quasi-electric field components are added in Eqs. (10) and (11) as follows:

$$J_{ni} = \frac{\mu_{ni}}{h_1} \left[\frac{\Psi_0 - \Psi_1 + \omega_0 - \omega_1}{1 - \exp(\Theta_n(\Psi_0 - \Psi_1)) \exp(-\Theta_n(\omega_0 - \omega_1))} n_0 + \frac{\Psi_0 - \Psi_1 + \omega_0 - \omega_1}{1 - \exp(-\Theta_n(\Psi_0 - \Psi_1)) \exp(\Theta_n(\omega_0 - \omega_1))} n_1 \right] \quad (12)$$

$$J_{pi} = \frac{\mu_{pi}}{h_1} \left[\frac{\Psi_0 - \Psi_1 - \omega_0 + \omega_1}{1 - \exp(-\Theta_p(\Psi_0 - \Psi_1)) \exp(\Theta_p(\omega_0 - \omega_1))} p_0 + \frac{\Psi_0 - \Psi_1 - \omega_0 + \omega_1}{1 - \exp(\Theta_p(\Psi_0 - \Psi_1)) \exp(-\Theta_p(\omega_0 - \omega_1))} p_1 \right] \quad (13)$$

where

$$\omega = \frac{kT}{q} \ln\left(\frac{n_i}{n_i^0}\right)$$

Here, n_{ie} and n_i are the effective intrinsic carrier and intrinsic carrier concentrations. Each discretized equation is solved, using Stone's strongly implicit procedure (SIP) [10]. For SIP parameters for current continuity equations, zero values are used. These discretized equations are simultaneously solved by Gummel's iterative method [8]. The convergence of non-linear iteration is judged with δ of Eq. (6).

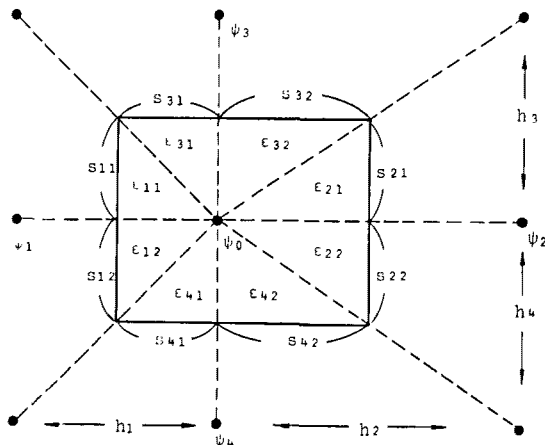


Fig. 4 Cell with eight triangular subregions in rectangular grids

4.2 The method setting initial conditions

The initial conditions for the numerical solution of Eq. (6) are prepared by depletion layer analysis or by extrapolation. In depletion layer analysis, Poisson's equation is simplified as

$$\nabla(\epsilon \nabla \psi) = -q \Gamma - Q_{ss} \quad (14)$$

in insulator and depletion layer of semiconductor. The constant value of ψ is used in other regions of semiconductor. Equation (14) is solved with the successive overrelaxation. This method does not require an initial condition for itself, and can be used to approximate solutions of Poisson's equation for any device structure. DSS estimates the electrostatic potential by extrapolation if the electrode voltage changes successively during simulation, for example, calculation of I-V characteristics. The changes in electrostatic potential distributions are estimated from the electric field for the latest solutions in successive simulations. The initial conditions for electron and hole concentrations are calculated from electrostatic potential and fermi levels on the ohmic electrodes.

Boundary conditions are given as hold values for ohmic electrode and Schottky electrode. The conditions of charge neutrality and thermal equilibrium are applied to ohmic electrodes. Interpolation method, one dimensional solution, and free boundary can be also set.

4.3 Physical models

DSS uses the physical models as shown below. Avalanche generation (G), bulk Shockley-Read-Hall recombination (R_{SHR}), and Auger recombination (R_A) are modeled using the equations as follows:

$$G = \alpha_n k_1 |n_1| + \alpha_p |J_p| \quad (15)$$

$$R = R_{SHR} + R_A \quad (16)$$

$$R_{SHR} = (np - n_i^2) / [\tau_n(p + p_1) + \tau_p(n + n_1)] \quad (17)$$

$$R_A = (np - n_i^2)(C_n n + C_p p) \quad (18)$$

where p_1 , n_1 , C_n , and C_p are parameters. α and τ are the ionization rate [11] and carrier lifetime, respectively, given by

$$\alpha = A \exp(-B|J| / |E \cdot J|) \quad (19)$$

and

$$\tau = \tau_{min} + (\tau_{max} - \tau_{min}) / (1 + (\Gamma / \Gamma_0)^\beta) \quad (20)$$

Here, A , B , τ_{min} , τ_{max} , β , and Γ_0 are parameters. At the surface, surface Shockley-Read-Hall model (R_s) is expressed by

$$R_s = (n_p - n_i^2) / [(p + p_0) / S_n + (n + n_0) / S_p] \quad (21)$$

where S_n and S_p are parameters. The effective intrinsic carrier concentration due to the effect of bandgap narrowing[12] is expressed as

$$n_{ie} = n_i \exp\left(\frac{kT}{2q} \left(\ln \frac{V_1}{N_0} + \sqrt{\left(\ln \frac{V_1}{N_0} \right)^2 + C} \right)\right) \quad (22)$$

where N_0 , V_1 , and C are parameters. The relationship(13) between diffusivity and mobility is approximated by

$$\frac{1}{\Theta} = \frac{D}{\mu} = \frac{kT}{q} \left[1 + \frac{\sqrt{3}}{4} \left(\frac{n_c}{N_c} \right) - 2 \left(\frac{3\sqrt{3}}{16} \right) \left(\frac{n_c}{N_c} \right)^2 \right] \quad (23)$$

where n_c and N_c are the carrier concentration and parameter, respectively. Carrier mobility models use Scharfetter and Gummel's expression[9] including Thornber's scaling law[14] for bipolar devices and Yamaguchi's model[15] for MOS devices, respectively.

$$\mu = \mu_{NE} \sqrt{1 + \frac{(\mu_{NE} E_{\parallel} / v_0)^2}{(\mu_{NE} E_{\parallel} / v_0 + F)^2} + (\mu_{NE} E_{\perp} / v_0)^2} \quad (24)$$

where

$$\mu_{NE} = \mu_0 \sqrt{1 + \Gamma / (\Gamma + S + N_r)} \quad (25)$$

for bipolar devices, and

$$\mu_{NE} = \mu_0 \sqrt{(1 + \Gamma / (\Gamma + S + N_r))(1 + E_{\perp} / E_{\parallel})} \quad (26)$$

for MOS devices. Here, E_{\perp} and E_{\parallel} are components of the electric field perpendicular and parallel to the current density vector, and v_0 , v_s , S , N_r , E_0 and μ_0 are parameters.

5. APPLICATIONS OF THE DEVICE SIMULATION

The device simulation program with the free step design method was tested with various semiconductor devices.

Typical n-channel MOSFETs were first simulated under the simulation procedure as shown in Table 1. This device has a gate length of 2.0 microns, a gate oxide thickness of 0.03 microns, and the junction depth of 0.3 microns under the source and drain electrodes. DSS receives both data of device structure as shown in Fig. 3 and a sequence of six steps from PPDS, and operated as stated below. In the first step, the Poisson's equation is solved rapidly by depletion layer analysis. Electron concentration and electrostatic potential are analyzed to approximate the true solutions. Next, the hole concentration, generation, and recombination are included into the simulation. In the last step, the electron and hole concentrations are solved to enhance the accuracy of the electrode currents. The bandgap narrowing effect, and the

Einstein relation for degenerate carrier concentration are not used in this simulation.

Figure 5 shows the I-V characteristics obtained according to this procedure. Solid lines and circles are experimental data and simulation results, respectively. The simulation results are in good agreement with experimental data when the coefficient of E_0 in Eq. (26) is fitted at one point in the saturation region. This program can be simulated by two-carrier analysis under the condition of avalanche breakdown. Computation time per bias point was about 3 minutes for a 3-MIPS computer where the number of nodes was 1800 points, and the gate, drain, and substrate voltages were 3.0, 4.0 and 0.0 volts, respectively.

Figure 6 shows the dependence of the drain current on the minimum vertical grid interval. The drain currents increase due to the discretization error as the grid interval widens. This error is negligible for intervals of less than 10 angstroms. The discretization error for horizontal grid interval was also investigated and found independent of the interval.

Figure 7 shows the distribution on the electrostatic potential, both electron and hole concentrations and generation rate in the avalanche phenomena for $V_{GS} = 4.0V$, $V_{DS} = 7.5V$, and $V_{BS} = 0V$. Figure 8 shows the electrostatic distribution in the n-channel MOSFET with four gate electrodes, which is a delay line in the CCD sensor. DSS uses step design for one-carrier analysis as shown in Table 2 because this device is operated in the bias condition where the static currents do not occur. In this case, DSS was executed with a computation time of less than 1 minute, which is comparable to the speed of an exclusive simulator. Figure 9 shows the electrostatic potential distribution for a typical npn-bipolar transistor. The bandgap narrowing effect is considered in device simulation. This program was found useful for applications to various devices.

6. CONCLUSION

To realize a useful device simulation program for arbitrary device structure and general analysis it is important and effective that the device simulator is independent of the device structure. The pre-processor must operate the user interface exclusively. Device simulator performs numerical solution according to input data sent from the pre-processor. The input data is a sequence of design steps and informations about nodes and boundaries. In each design step, solved equations, physical models, and convergence conditions are specified. The combination of these steps enabled device simulation to find a better numerical solution in the less computation time. Depletion layer analysis was effective for setting initial conditions for numerical solution independent of the

104 device structure. The device simulation program developed with the algorithms above proved to be applicable to many devices, and expected to be used in the research and development of VLSI devices.

Table 1
Step designs for n-channel MOSFET

STEP	VARIABLE	PHYSICAL MODEL	CONVERGENCE CONDITION
1	ψ		$\Delta\psi = 10^{-2}V$
2	ψ, n		$\Delta\psi = 10^{-3}V$
3	ψ, n, p		$\Delta\psi = 10^{-3}V$
4	ψ, n, p	G	$\Delta\psi = 10^{-4}V$
5	ψ, n, p	G, R	$\Delta\psi = 10^{-4}V$
6	n, p	G, R	$\frac{\Delta n}{n} = \frac{\Delta p}{p} = 10^{-5}$

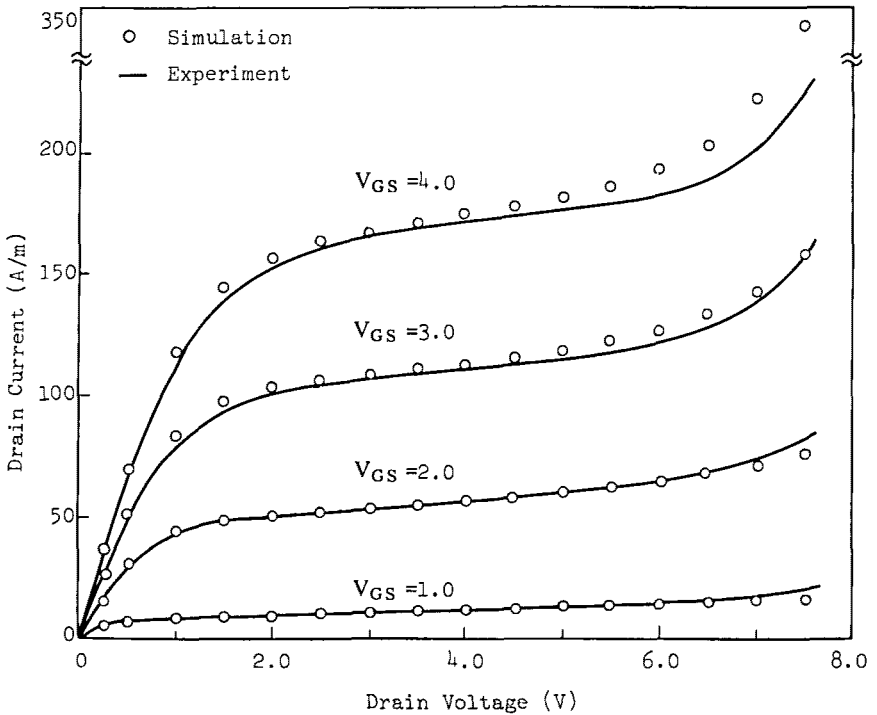


Fig. 5 I-V characteristics of n-channel MOSFET (Substrate voltage is 0.0V.)

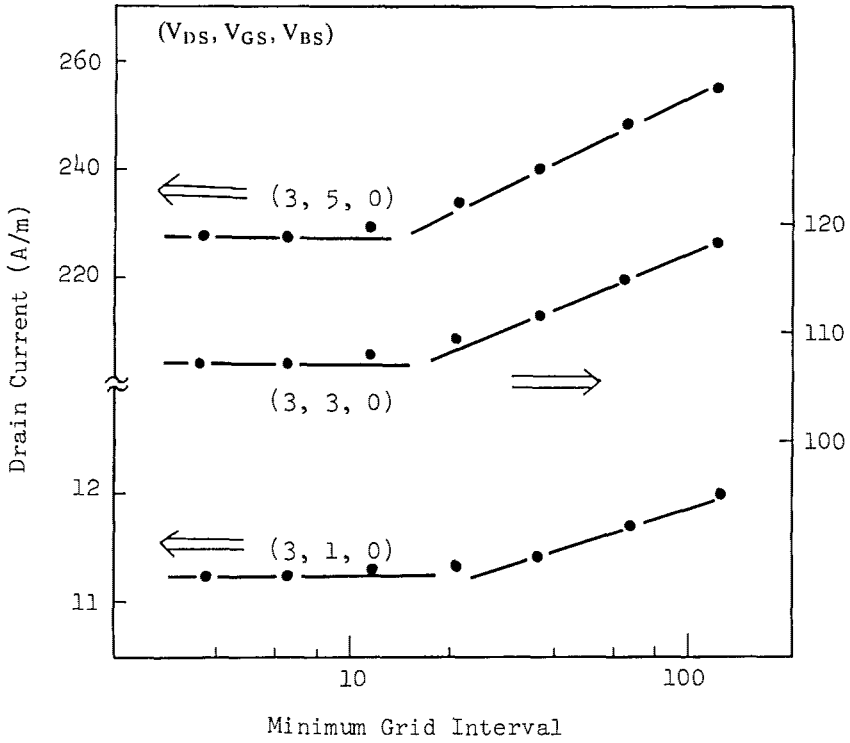
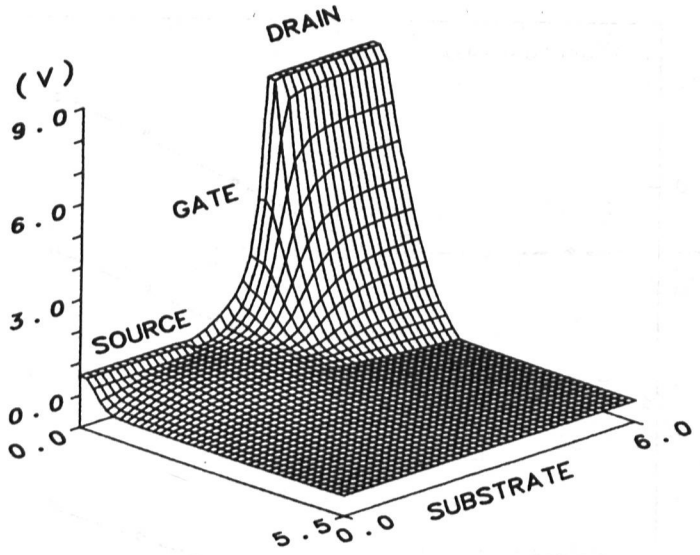
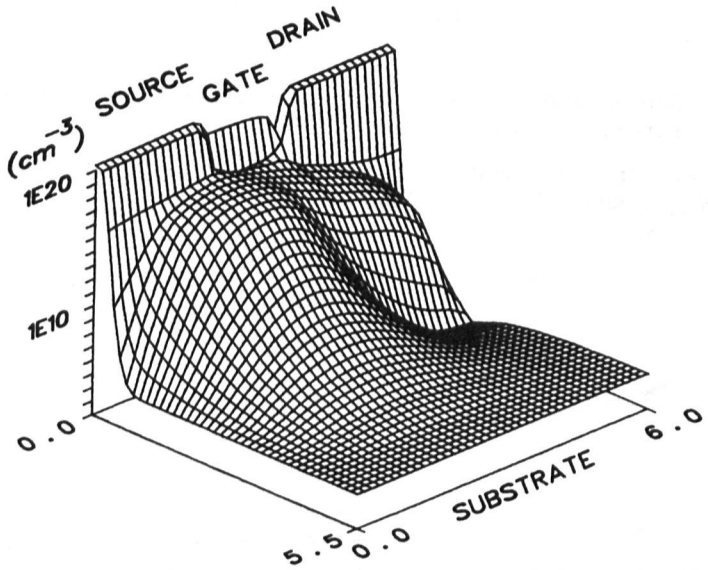


Fig. 6 Dependence of drain current on minimum vertical grid interval for n-channel MOSFET

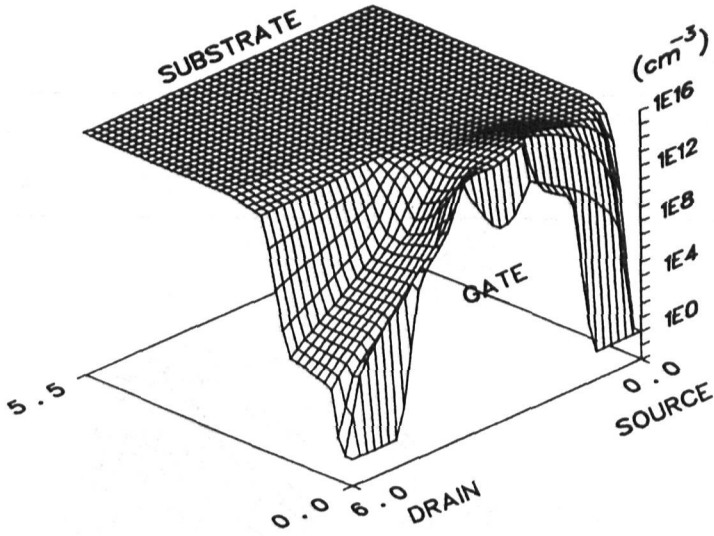
Parameters in the figure show the voltages at drain (V_{DS}), gate (V_{GS}), and substrate (V_{BS}), respectively.



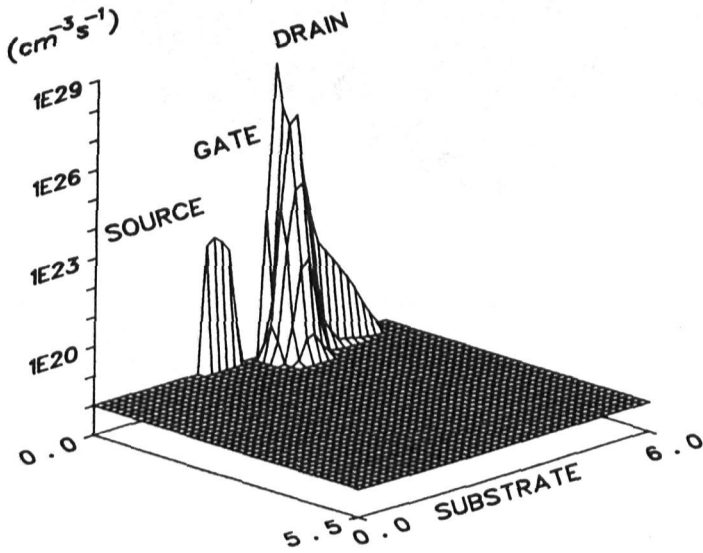
(A) Electrostatic potential distribution



(B) Electron concentration distribution



(C) Hole concentration distribution



(D) Generation rate distribution

Fig. 7 Avalanche phenomena in the n-channel MOSFET at $V_{GS}=4.0V$, $V_{DS}=7.5V$, and $V_{BS}=0.0V$

Table 2

Step designs for n-channel MOSFET with four gate electrodes

STEP	VARIABLE	PHYSICAL MODEL	CONVERGENCE CONDITION
1	ψ		$\Delta\psi = 10^{-2}V$
2	ψ, n		$\Delta\psi = 10^{-4}V$

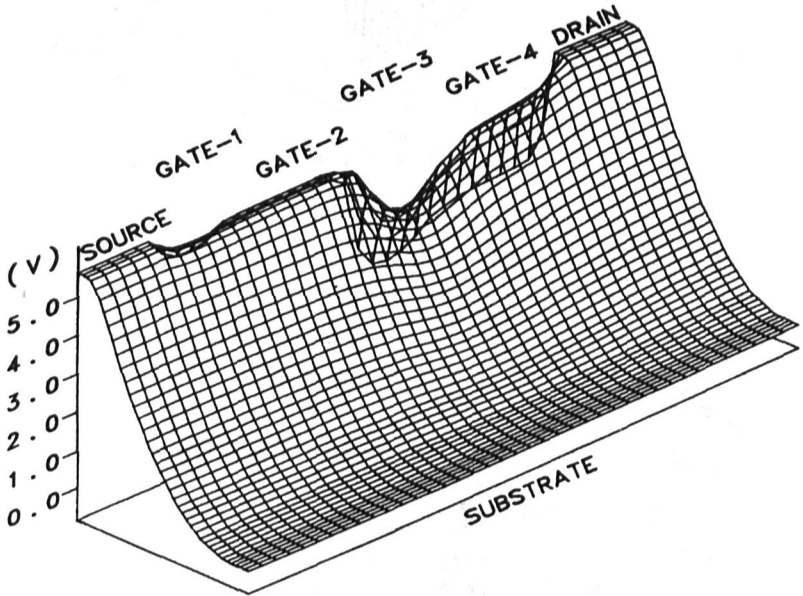


Fig. 8 Electrostatic potential distribution in n-channel MOSFET with four gate electrodes where $V_{DS}=0.1V$, $V_{GS1}=-1.0V$, $V_{GS2}=-1.0V$, $V_{GS3}=-4.0V$, $V_{GS4}=-4.0V$, and $V_{BS}=-5.0V$, respectively.

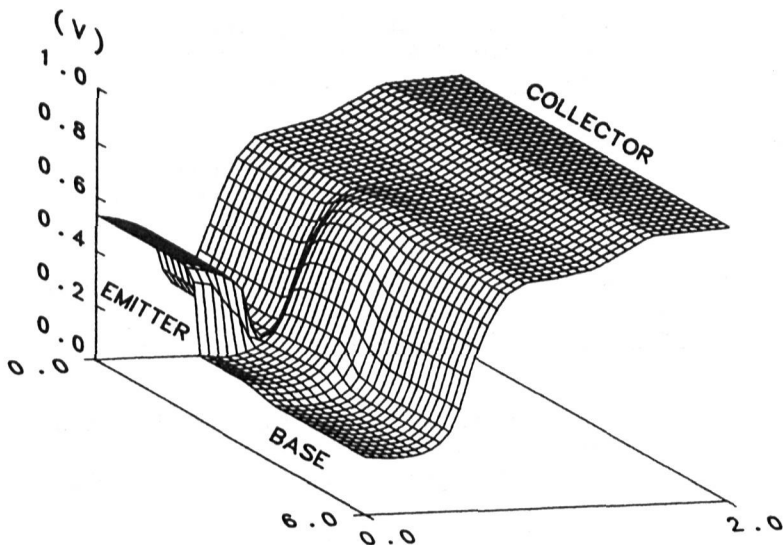


Fig. 9 Electrostatic potential distribution for typical npn-transistor where $V_{BE}=0.7V$ and $V_{CE}=0.5V$.

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REFERENCES

1. Mock, M.S.
"A two-dimensional mathematical model of the insulated-gate field-effect transistor"
Solid-State Electron., vol. 16, p. 601, 1973.
2. Toyabe, T. and Asai, S.
"Analytical models of threshold voltage and breakdown voltage of short-channel MOSFET's derived from two-dimensional analysis"
IEEE J. Solid-State Circuits, vol. SC-14., p. 375, 1979.
3. Sano, E., Kasai, R., Ohwada, K. and Ariyoshi, H.
"A two-dimensional analysis for MOSFET's fabricated on buried SiO₂ layer"
IEEE Trans. Electron Devices, vol. ED-27, p. 2043, 1980.
4. Engl, W.L., Dirks, H.K. and Meinerzhagen, B.
"Device modeling"
Proc. IEEE, vol. 71, p. 10, 1983.

5. Selberherr, S., Schütz, A. and Pötzl, H.W.
"MINIMOS-A two-dimensional MOS transistor analyzer"
IEEE Trans. Electron Devices, vol. ED-27, p. 1540, 1980.
6. Watanabe, D.S. and Slamet, S.
"Numerical simulation of hot-electron Phenomena"
IEEE Trans. Electron Devices, vol. ED-30, p. 1042, 1983.
7. Nishi, K., Sakamoto, K. and Ushio, S.
"Process simulation of multilayer structures involving polycrystalline and silicon nitride"
Ext. Abstr. ECS Fall Meeting 1981 Denver, p. 998, 1981.
8. Gummel, H.K.
"A self-consistent iterative scheme for one-dimensional steady state transistor calculations"
IEEE Trans. Electron Devices, vol. 11, p. 455, 1964.
9. Scharfetter, D.L. and Gummel, H.K.
"Large-signal analysis of a silicon read diode oscillator"
IEEE Trans. Electron Devices, vol. ED-16, p. 64, 1969.
10. Stone, H.L.
"Iterative solution of implicit approximations of multi-dimensional partial differential equations"
SIAM J. Numer. Anal., vol. 5, p. 530, 1968.
11. Grant, W.N.
"Electron and hole ionization rates in epitaxial silicon at high electric fields"
Solid-State Electron., vol. 16, p. 1189, 1973.
12. Slotboom, J.W. and De Graaff, H.C.
"Measurements of bandgap narrowing in Si bipolar transistors"
Solid-State Electron., vol. 19, p. 857, 1976.
13. Kroemer, H.
"The Einstein relation for degenerate carrier concentrations"
IEEE Trans. Electron Devices, vol. ED-25, p. 850, 1978.
14. Thornber, K.K.
"Relation of drift velocity to low-field mobility and high-field saturation velocity"
J. Appl. Phys., vol. 51, p. 2127, 1980.
15. Yamaguchi, K.
"A mobility model for carriers in the MOS inversion layer"
IEEE Trans. Electron Devices, vol. ED-30, p. 658, 1983.