COMPUTER MODELLING OF TRAVELLING WAVE TRANSISTORS

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ABSTRACT

A theoretical model is presented which describes the performance of all basic semiconductor travelling wave devices. These include the travelling wave (or 'distributed') amplifier (TWA) and the travelling wave field effect transistor (TWF). The model includes all interelectrode and transistor intrinsic circuit elements and performs a full multi-line modal analysis. Calculations are reported which compare and contrast the performance of the TWA and TWF and the fundamental differences in their operation are explained.

1. INTRODUCTION

Interest in travelling wave semiconductor devices has been growing and two distinct areas have emerged, distinguished under the headings: Travelling Wave Amplifiers [1,2,3] (TWA) and Travelling Wave Field Effect Transistors [4,5,6,7] (TWF). The devices may be considered as 'active' transmission lines and, with modifications, show the potential of medium power (500-1000 mW) broad-band width operation[2,7].

The design of these devices relies heavily on theoretical models which take into account distributed effects and transmission modes within the device. All the models published to date have been specific, either to the TWA [1-3] or to the TWF [4-6] and have generally given incomplete descriptions of inter-electrode coupling, mode analysis and parasitic effects.

This paper reports an extension of recent work at Plessey, Caswell, on the TWF (to be published elsewhere [7]), which has led to a unified model describing both TWF and TWA.

2. PHASE BALANCE

The traditional problem in travelling wave operation is to

balance the phase on the gate and drain electrodes so as to continue to drive the transistors along the entire width of the device [1-7]. The source-gate capacitance is large compared with the drain-source capacitance and if we view the gate and drain electrodes as independent transmission lines with the source-earthed geometry, then the difference in capacitance will make waves on the gate line travel more slowly than waves on the drain line. In practice the problem is more complicated but when properly analysed [7], it is still clear that compensation is needed. The TWF and TWA differ in the way they achieve this compensation. For the TWF additional capacitance is loaded onto the drain line, either by direct overlays [6.7] or by a novel image gate arrangement [4]. Compensation in the TWA is effected by making the drain transmission line longer than the gate transmission line between active elements [1].

3. MODEL

If we compare the practical and theoretical results of Ayasli et al [1] and Holden et al [7] we find that the TWA design yields a better gain-bandwidth product than the TWF design for total gate widths of less than 2 to 3 mm and at low frequencies (2 to 12 GHz). To understand this result a common model must be used which applies equally well to both types of device. Our TWF model [7] takes a distributed equivalent circuit together with an ab-initio evaluation of the mutual capacitance and inductance of the transmission lines to form 3 x 3 admittance and impedance matrices Y and Z respectively (see Fig.1). These are evaluated 'per unit length' of the three coupled transmission lines (source, gate and drain).

Applying suitable boundary conditions for the matching circuitry produces the total solution giving overall gain response [7].

This model is sufficient for the TWF but for the TWA the equations have to be modified to allow for different lengths of gate and drain transmission line. This is achieved by a generalisation of the method of Ayasli et al [1], and is described in the appendix. Displacements along the gate (and source) transmission lines are scaled to the displacement along the drain line by the ratio of l_g (or l_s) to l_d (here l_g, l_s and l_d are the unit lengths of gate, source and drain transmission lines between active Fet elements, see Fig.2). The drain displacement becomes the common translation variable and maps to corresponding points on gate and source.

It is assumed that all lumped circuit elements in the transistors and coupling between transmission lines can be treated as distributed over the whole line unit of the corresponding transmission line, a satisfactory approximation provided

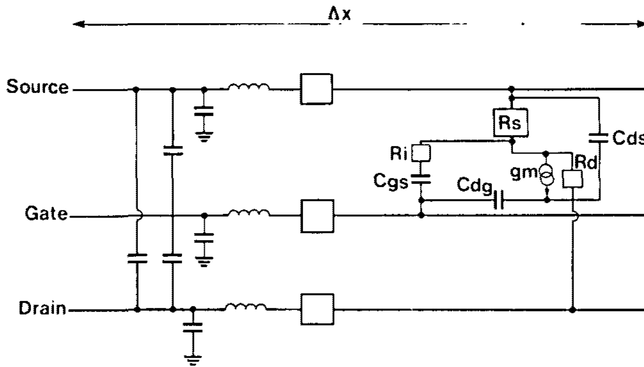

Fig.1. Differential element of the distributed coupled transmission line circuit showing the geometrical and active FET elements. Some components have been omitted for clarity.

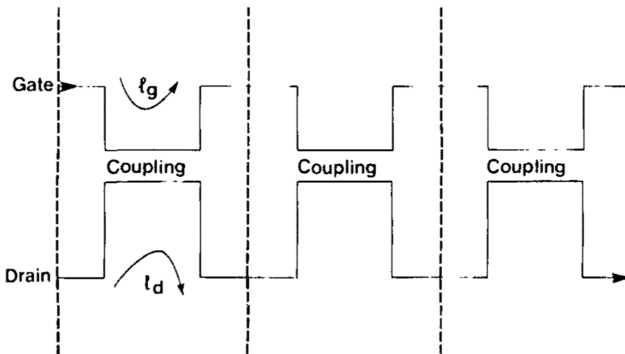

Fig.2. Schematic diagram of the coupled, meandered electrode arrangement. The active devices are inserted in the 'coupling' regions.

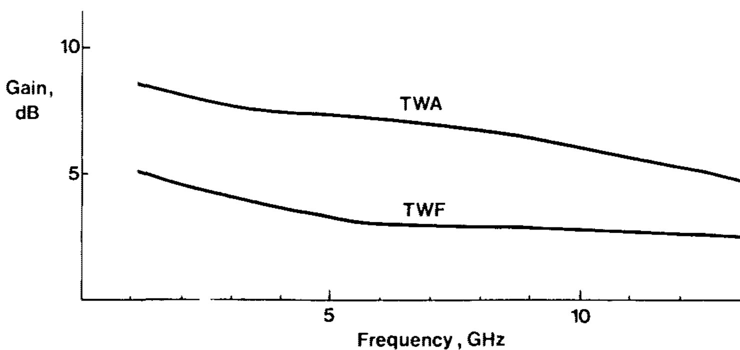

Fig.3. Comparison of the simulation results for a TWA and TWF. Both arrangements have active devices of one micron gate length (see Table 1) with a total active gate width of 2 mm.

that the line unit is significantly shorter than the wavelength of interest. Fig.2 illustrates the model. The key improvements over the Ayasli et al [1] work are that all the standard equivalent circuit elements are included and scaled to their respective transmission lines (as are direct interelectrode coupling elements), and a full coupled line modal analysis is carried out. The scaled transmission line equations are solved as before and the model allows all TWF and TWA designs to be analysed.

4. RESULTS

Typical theoretical gain curves for the two types of device are shown in Fig.3. For comparison the same basic equivalent circuit (for a 1 micron gate length device) is used in each, together with the same overall active gate width (2 mm). The drain meander in the TWA and compensating source-drain capacitance in the TWF are optimised for maximum gain in each case. Equivalent Circuits Data for the TWA and TWF used in the simulation for Fig.3 are given in Table 1. Note that the geometry of the microstrip electrodes in the coupling region is the same in both devices with source and drain electrodes 50 microns wide and gate electrode 10 microns wide (in the TWF a 'mushroom' cross-section is assumed to lower gate resistance). The comparison is not however very sensitive to geometry. In the TWA the drain line is optimised to be 3.5 times longer than the gate. In the TWF the 2mm of active gate widths are assumed to be distributed continuously along 2 mm of transmission line. In the TWA this total width is made from 5 units of 400 microns of active gate connected by transmission devices in the appropriate length ratio. The active coupling region between the microstrip lines (l_a - see appendix) is taken to be 400 microns but this is not critical. Source and gate element lengths (l_s and l_g - see appendix) are set equal for convenience. The source length is again not critical and although the source is assumed to be a continuous parallel line in our simulation this is not essential and source pads - as used in existing TWAs should give similar results. It is clear from the figure that the TWA geometry gives better gain in this frequency range, for the same total active gate-width.

5. METHODS OF OPERATION

One advantage of the full modal analysis is that all the eigenmodes are generated for each device structure. Inspection of the normal modes which propagate in each of the structures shows that the devices work in completely different ways. The TWF has two lossy modes and one showing strong exponential gain [4-7] (a negative imaginary part of the propagation constant). This third mode is a balanced wave with approximately +V volts on the gate, -V volts on the drain and zero volts on the source.

TABLE 1 - EQUIVALENT CIRCUIT PARAMETERS (See Figure 1)

PARAMETER	DESCRIPTION	TWA	TWF
$Rs/\Omega m$	Intrinsic Source Resistance	$1x10^{-3}$	$1x10^{-3}$
gm/Sm^{-1}	Magnitude of Intrinsic Transconductance	100	100
τ/s	Transit Time	$4x10^{-12}$	$4x10^{-12}$
Cds/Fm^{-1}	Intrinsic Source-drain	$5x10^{-13}$	$5x10^{-13}$
Rds/Fm^{-1}	ditto	$1x10^{-3}$	$1x10^{-3}$
$Rd/\Omega m$	Drain Resistance (See Figure 1)	0.2	0.2
Cdg/Fm^{-1}	Intrinsic gate-drain	$6x10^{-11}$	$6x10^{-11}$
Cgs/Fm^{-1}	Source-gate 'Depletion'	$1.2x10^{-9}$	$1.2x10^{-9}$
$Ri/\Omega m$	Channel Resistance	$1.25x10^{-3}$	$1.25x10^{-3}$
ADDITIONAL PARASITICS			
$R_{DD}/\Omega m$	Source-Source Electrode and Drain to Drain Electrode	$4x10^{-6}$	$4x10^{-6}$
$RS/\Omega m^{-1}$	Electrode Resistances	1000	1000
$RG/\Omega m^{-1}$		4000	7000
$RD/\Omega m^{-1}$		500	500
$C1/Fm^{-1}$	Gate → Drain Capacitance due to T Cross-section Gate	0.0	0.0
$C2/Fm^{-1}$	Gate-Source Capacitance due to T Cross-section Gate	$0.35x10^{-9}$	$0.35x10^{-9}$
$C3/Fm^{-1}$	Balancing Overlay Capacitance Source to Drain	$1.1x10^{-9}$	0.0
$RBW/\Omega m$	Source-earth Bond Wire Resistance	$0.2x10^{-3}$	$0.2x10^{-3}$
$DINB/Hm$	Source-earth Bond Wire Inductance	$0.11x10^{-12}$	$0.11x10^{-12}$
	TOTAL ACTIVE GATE WIDTH	2mm	2mm

When launched with balanced feeds [7] this mode alone provides the gain in the device. The TWA has two important modes, each with +V volts on the drain and a smaller voltage on the gate which is positive in one mode and negative in the other. One mode has a very small loss component, the other mode has considerably higher loss. Driving the device at the input with +V volts on the gate and zero volts on the drain excites both modes equally but with opposite sign. The two large drain voltages are in opposition on the drain input producing zero volts whereas the gate voltages add. In travelling along the device the lossy mode is absorbed and a large voltage is left on the drain output yielding gain. This combination of low and high loss modes is typical of conventional FET structures and is essential to their giving gain [8]. The gain available from the TWA is thus limited. Once the device is significantly wider than the characteristic decay length of the lossy mode no further improvement occurs. The TWF on the other hand has no such restriction as its 'growing wave' will continue to grow as the device is widened and so may find application at gate widths in excess of 10 mm. However, the usable width of the TWF is also limited because its reciprocal nature enhances 'Fabry-Perot' oscillations caused by mismatched boundaries [7]. These arise because the growing wave, on reflection from the boundary, continues to grow on its return leading to large resonant gain and possible instability.

THE PHYSICAL DIFFERENCE BETWEEN THE TWA AND TWF

The physical reason why the TWA gives more gain from 2 mms of active gate than the TWF is connected with the higher characteristic impedance of the TWA. Although the simple TWA theory [1] is inappropriate for the TWF it is a useful analytical tool to illustrate the differences. Following Ayasli et al [1] and using their notation the condition for 'compensated' wave operation (equal phase velocity on each line) is:

$$l_g \sqrt{L_g \left(C_g + \frac{C_{sg}}{l_g}\right)} \simeq l_d \sqrt{L_d \left(C_d + \frac{C_{ds}}{l_d}\right)} \qquad (1)$$

where L_g (L_d) and C_g (C_d) are the inductance and capacitance per unit length on the gate (drain) transmission lines, C_{sg} and C_{sd} are the distributed depletion and source-drain capacitances for the active FETs ($C_{sg} > C_{sd}$) and l_g, l_d are as defined in Fig.2. It can argued that, in the TWA, (1) is satisfied by making $l_d > l_g$ and in the TWF (1) is satisfied by keeping $l_d = l_g$ but increasing the value of C_{ds}. From Ayasli et al [1] (equation (5)) the gain in the device is

$$G = \frac{g_m^2 n^2 Z_d \ Z_g}{4} \qquad (2)$$

where n is the number of FET elements with transconductance g_m and where

$$Z_g \simeq \left[\frac{L_g}{C_g + \frac{C_{gs}}{l_g}}\right]^{\frac{1}{2}} \quad (3)$$

and

$$Z_d \simeq \left[\frac{L_d}{C_d + \frac{C_{ds}}{l_d}}\right]^{\frac{1}{2}} \quad (4)$$

are the transmission line impedances.

From (4) it is clear that $Z_d(TWF) < Z_d(TWA)$ which leads to higher gain in the TWA through (2) and a higher impedance for matching to external circuitry.

It must be stressed that the above analysis is only an illustration, however, our full modal analysis supports the general conclusions as demonstrated by Fig.3.

CONCLUSIONS

We conclude that the TWA and TWF are fundamentally different devices in that the TWA produces gain in a conventional manner whereas the TWF shows a novel growing wave mode. The consequences of this are that the TWF has potential for higher gain at greater gate widths but at gate widths currently attainable the higher impedance of the TWA gives it a better gain bandwidth product and more suitable characteristics for matching to currently available external circuitry. Our new mathematical model is the first to combine a full description of the geometrical microstrip coupling and the equivalent circuit of the FET within a three coupled line modal analysis. The extension described in this paper encompasses the alternative phase balance option of meandered transmission lines and thus allows a direct comparison to be made between all types of travelling wave semiconductor device.

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APPENDIX

With reference to Figure 1 three coupled transmission line equations can be derived in terms of general impedance and admittance matrices. The equal line length case is discussed in reference [7]. In this appendix we further generalise the calculation to account for differences in the line length of source gate and drain electrodes between active units (shown schematically in Figure 2). We confine the interline coupling to 'common' sections of line of lengths la. These 'active sections' form part of the overall length of each line within one repeat unit (within the dotted lines in Figure 2) defined as ls, lg and ld for the source, gate and drain electrodes respectively. Finally within the spirit of travelling wave device theory we treat this 'lumped' coupling in the region la as if it were spread evenly along the whole unit length of each line this is a generalisation of the method used by Ayasli [1]. For example if the admittance per unit length in the active region, between the gate and drain lines is A_{23} this appears on the gate line as a distributed admittance $(la/lg)A_{23}$ and on the drain lines as $(la/ld)A_{23}$.

To define the appropriate voltage level at each line we map points on the gate or source lines to points on the drain line by scaling. If a position on the drain line is represented by the variable x then the mapped position measured along gate and source will be $(lg/ld)x$ and $(ls/ld)x$ respectively. Thus our example distributed admittance A_{23} will connect the gate electrode voltage evaluated at $(lg/ld)x$ along the gate line and the drain voltage evaluated at x along the drain line.

It is convenient to begin by ignoring the active intrinsic circuit and derive the passive coupled line equations. Generalising the standard transmission line procedure we apply Kirchoffs voltage law to each line in turn using the scaling and mapping described above. We use the subscript 1, 2, 3 to denote source gate and drain lines and arrive at the general form

$$V_1\left(\frac{xls}{ld}\right) - V_1\left((x+\Delta x)\frac{ls}{ld}\right) = \Delta x \frac{ls}{ld}\left[Z_{11}\, I_1\left(\frac{xls}{ld}\right) + Z_{12}\frac{la}{ls}\, I_2\left(\frac{xlg}{ld}\right) + Z_{13}\frac{la}{ls}\, I_3\left(\frac{xld}{ld}\right)\right] \qquad (A1.1)$$

with two similar equations for the gate and drain with suitable permutations of ls, lg and ld. Here Z_{ij} are the impedances per unit length between lines i and j. Note that the diagonal impedances are not scaled to the active regions la because they represent inductance and resistance of the lines along the whole unit length. The appropriate currents multiplying the material inductances are evaluated at the appropriate scaled point on the coupled line.

Taking the limit of $\Delta x \to 0$ we obtain

$$- \frac{dV_1}{dx} = \left[Z_{11} \frac{ls}{ld} \quad I_1 \left(\frac{xls}{ld}\right) + Z_{12} \frac{la'}{ld} \quad I_2 \left(\frac{xlg}{ld}\right) + Z_{13} \frac{la}{ld} \right.$$

$$\left. I_3 \left(\frac{xld}{ld}\right) \right] \tag{A1.2}$$

with similar equations for gate and drain.

Similarly we can apply Kirchoffs current law to each node and obtain a corresponding set of equations in the admittances A_{ij},

$$\frac{-dI_1}{dx} = \left(A_{11} \frac{ls}{ld} + A_{12} \frac{la}{ld} + A_{13} \frac{la}{ld}\right) V_1 \left(\frac{xls}{ld}\right) - A_{12} \frac{la}{ld}$$

$$V_2 \left(\frac{xlg}{ld}\right) - A_{13} \frac{la}{ld} \quad V_3 \left(\frac{xld}{ld}\right) \tag{A1.3}$$

with appropriate permutations for gate and drain.

By an obvious definition of a matrix $\underset{\approx}{Y}$ we can write the set of equations (A1.3) as the matrix equation

$$- \frac{d\underline{I}}{dx} = \underset{\approx}{Y} \, \underline{V} \tag{A1.4}$$

where $\underline{I}$ and $\underline{V}$ are current and voltage vectors whose components represent the currents and voltages on each line evaluated at the appropriate scaled points.

With an obvious revised definition of the matrix $\underset{\approx}{Z}$ the set of equations (A1.2) can be written in the matrix form:

$$- \frac{d\underline{V}}{dx} = \underset{\approx}{Z} \, \underline{I} \tag{A1.5}$$

Equations (A1.4) and (A1.5) are a generalisation of the familiar transmission line equations to the case of multiple coupled lines of differing length. With the above prescription for scaling and performing the Kirchoff sums the additional distributed elements of the equivalent FET circuit (as shown in Figure 1) can be included. Equation (A1.5) is unaffected but the additional current nodes in the circuit have to be taken into account in (A1.4). The process is messy but tractable and a new (A1.4) is produced where $\underset{\approx}{Y}$ becomes $\underset{\approx}{Y} + \underset{\approx}{Ya}$ with $\underset{\approx}{Ya}$ being the active admittance matrix which is in parallel with the 'geometrical' line admittances and therefore adds in a matrix form of the rule of addition of admittances in parallel.

To proceed further we choose a specific form for the wave
ions of the transmission line equations:

$\underset{\sim}{V}io \; e^{j(k_i x - wt)}$ (A1.6a)

The frequency dependence (w) is already included in the
ition of admittance and impedance. The k vector is our
ex propagation constant (note that this may differ from
definitions found in the literature).

$\underset{\sim}{V}io \; e^{jk_i x}$

lso

$\underset{\sim}{I}io \; e^{jk_i x}$ (A1.6b)

Where $\underset{\sim}{V}i$ ($\underset{\sim}{I}_i$) is the eigenvector and $\underset{\sim}{V}io$ its magnitude.
ituting (A1.6b) into (A1.4) and (A1.5) in turn and elimin-
$\underset{\sim}{I}io$ yields

$io = [- \underset{\approx}{Z}\underset{\approx}{Y} \;] \; \underset{\sim}{V}io$ (A1.7)

$\underset{\approx}{Y}$ is now the sum of the active and passive admittances.

Equation (A1.7) is the matrix eigenvalue equation whose
ions are the propagation modes of the three coupled,
e, transmission lines. By solving for the eigenmodes and
ing appropriate boundary conditions the response of any
lling wave semiconductor device can be determined as
in detail in [7].