

Transient 2-D Simulation of Power Thyristors

G.A.FRANZ, A.F.FRANZ

Institut für Allgemeine Elektrotechnik
Abt. Physikalische Elektronik
TU Wien, Gußhausstraße 27, A-1040 Vienna, AUSTRIA

Abstract

To a steadily growing extent, numerical simulation models are utilized for the development and the design of semiconductor power devices. However, these simulation programs to date, are known only to be handled under strong restrictions. This paper presents a novel program system capable of simulating 2-D transient device behavior under various operating conditions. Automatic set up and refinement of the grid by equidistribution of the local discretization error has been found an obligatory prerequisite for computing high voltage characteristics with a reasonable amount of computer resources. For the time discretization an automatic time step control algorithm has been implemented. The new time step is calculated with a predictor-corrector method. Due to the possibly large variation of the solution during transient simulation it is necessary to introduce a "moving grid". This is accomplished by tracing the local discretization error, which is equidistributed by deleting and inserting grid points. As an example, the rate effect of two thyristor elements, one with an emitter short and one without, is calculated. The shorted device is not triggered at the assumed dU/dt whereas simulations of the equivalent device without the emitter short show firing.

Introduction

The optimum design of power thyristors requires the use of numerical analysis tools capable of simulating device behavior under various conditions. Special emphasis must be given to the transient simulation of such structures. A reasonable number of papers have been published presenting specific results /1/-/6/ but nevertheless, the strong coupling of the semiconductor equations in the case of high injection and the extreme operating points (high voltages or high current densities) have restricted the efficient use of these software tools for design engineers. We present an exact numerical 2-dimensional transient model with locally refined grid structures,

automatic adaption to the different stationary and transient operating points and time step control. Theoretical and algorithmic aspects will be explained first, followed by a discussion of the advantages over heuristic methods. These advantages have been noted by studying the influence of emitter shorts on the rate effect of power thyristors.

Theoretical aspects

The numerical analysis of semiconductor devices requires the solution of three partial differential equations (Poisson's equation and two continuity equations for electrons and holes, respectively). To aid us in these calculations, we used a recently developed simulation program BAMB1 (Basic Analyzer of MOS and BIpolar devices). BAMB1 allows for the simulation of unrestricted device geometries /7/ and considers arbitrary models of the physical parameters. With respect to power devices having a shallow highly doped emitter region and high voltage/high current operating conditions, the classical 2-D discretization methods employ a large number of grid points such that reasonable storage requirements are often exceeded. Therefore, we have developed a new concept for the discretization of the fundamental semiconductor equations, the so called "Finite Boxes" /7/. In this approach the usual rectangular pattern of grid points is no longer considered. Instead, the mesh is built up by rectangular cells which permit lines to terminate in any direction. Using this strategy the grid is set up and refined automatically by equidistribution of the local discretization error of Poisson's equation.

During the transient simulation, large local variations of the internal distributions may occur. Space charge layers are built up and removed thereby. As a result, the value of the local discretization error changes and is no longer equidistributed. To handle this problem, two alternatives exist: The first way is to create a very fine rigid grid which must guarantee a sufficiently accurate discretization for all possible variations of the solution. This method requires a large number of grid points for all time steps and is rather inefficient. On the other hand, it is simple to implement and therefore has been frequently used. The second possibility introduces a "Moving Grid", whereby the local discretization error is traced. The

mesh is adapted by deletion and insertion of points if the error exceeds a certain tolerance value. In this manner, the calculation is always accomplished with a minimum number of necessary points, saving a great deal of computation time. We use this method in connection with the "Finite Boxes"-grid: we need not shift the mesh lines running through the device as it must be done using a classical rectangular grid. Instead, the adaption of the grid can be restricted to small areas around the critical regions. Investigations of the turn-on and turn-off behavior of thyristors have provided these results: the steady state solution for $t=0$ is calculated on an optimum matching grid which has been automatically set up and refined. During the transient analysis the equidistribution of the local discretization error is ensured by inserting grid points. A deletion of mesh points has been found unnecessary due to the fact that the basic grid represents a configuration of a minimum number of points and because each deletion of grid points is accompanied with a regularization procedure which may possibly neutralize the savings.

As an example, we present the "Moving Grid" during the turn-off of a small GTO element. The overall dimensions are as follows: gate length: $280\mu\text{m}$, cathode length: $115\mu\text{m}$, distance between gate and cathode contact: $35\mu\text{m}$, wafer thickness: $450\mu\text{m}$. Fig.1 shows a section of the "Finite Boxes" grid $235\mu\text{m}$ wide and $90\mu\text{m}$ deep around the gate and emitter contacts for the steady state operating point on the on-characteristic. Due to the fact that the device is flooded by the electron-hole plasma the pn-junction, between p-base and bulk situated $30\mu\text{m}$ under the surface, can not be detected in the discretization (no space charge present). The average current density in this region is approximately $300\text{A}/\text{cm}^2$. The device is turned off by applying a negative voltage to the gate contact. 70ns after the turn-off has been initiated, a space charge region exists around the pn-junction beneath the gate. This in turn, causes an insertion of grid points there (fig.2). As this layer extends towards the emitter, the grid points trace this movement as can be clearly seen in fig.3 at $t=120\text{ns}$.

The "Moving Grid" method is enhanced by an automatic time step control algorithm. We use a backward Euler method for the transient solution of the semiconductor equations, which implies no methodological restriction on the time step. Nevertheless, accuracy as well as convergence properties are highly influenced by the choice of the step

"MOVING GRID"

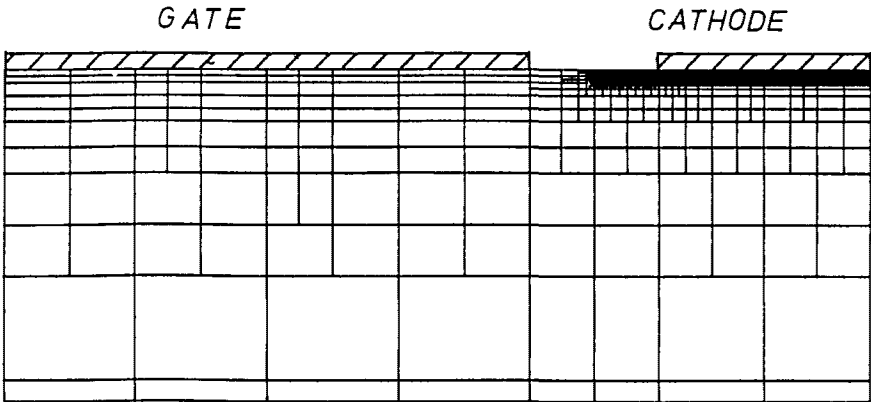


Fig 1: Section of a "Finite Boxes" grid (235 μ m \times 90 μ m) for a GTO-element at t=0.

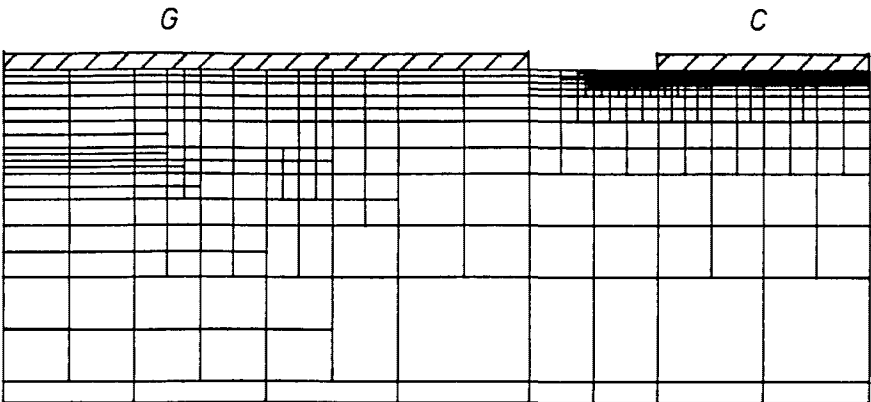


Fig 2: Section of a "Finite Boxes" grid for a GTO-element at t=70ns.

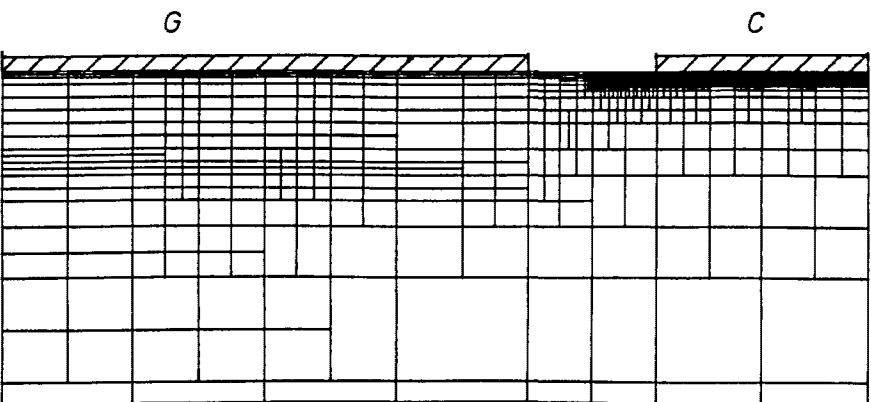


Fig 3: Section of a "Finite Boxes" grid for a GTO-element at t=120ns.

width. Heuristic methods seem to be widespread, e.g. /2/, /3/, but more generalized software tools like BAMBI can not rely upon such methods. To achieve maximum flexibility, we have developed an automatic time step control algorithm. The new time step is calculated with a predictor-corrector method based on changes of the space charge in the device. We start with an initial step derived from the minimum carrier life-time. If the space charge change is reasonably small, the new time step can be up to twice as large as the old one. If this space charge change increases during transient analysis, the time increment is decreased. In the case of poor convergence, the actual time step, Δt_n , is dropped and the calculation is restarted from t_{n-1} with a smaller increment. Since the fully implicit method causes a Newton iteration at each time step we need an initial guess. As suggested in /8/, it is derived by linear extrapolation of the previous two solutions at t_{n-1} and t_{n-2} . The combination of the "Moving Grid" together with the automatic time step control has proved to be stable. Nothing about the transient behavior of the device has to be known prior to the simulation. The described algorithms trace the solution and adapt the discretization parameters automatically.

Results - The rate effect in power thyristors

Two thyristor elements have been analyzed, one with an emitter short and one without. Both devices exhibit cylindrical symmetry, which allows for quasi three dimensional treatment after reformulation of the basic semiconductor equations in cylindrical coordinates /9/. Fig.4 shows the geometry of the device. The cathode contact is assumed to be a circular area with $96\mu\text{m}$ radius. Fig.5 is a plot of the assumed doping profile. The n^+ -emitter is very shallow ($3\mu\text{m}$) with a surface concentration of $2 \cdot 10^{20} \text{cm}^{-3}$. We have studied the influence of a rapid dU/dt -rate upon the performance of the thyristor element. A steep ramp voltage has been applied to the anode :

$$U_A = 1000 \text{ V}/\mu\text{s} \cdot t$$

The unwanted dU/dt triggering is usually prohibited by shorting the pn-junction between n^+ -emitter and p-base. The two devices considered here allow for the simulation of this effect. Device 1 is assumed to have a floating gate, whereas in device 2 the gate and cathode contacts are shorted. Fig.6 shows the anode current-versus-

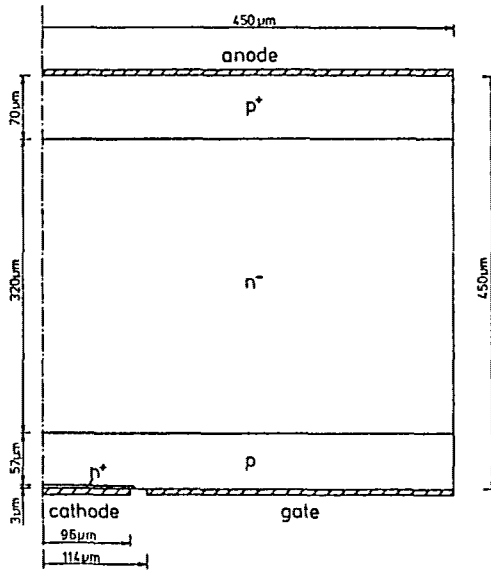


Fig 4: Simulation domain for the analyzed thyristor.

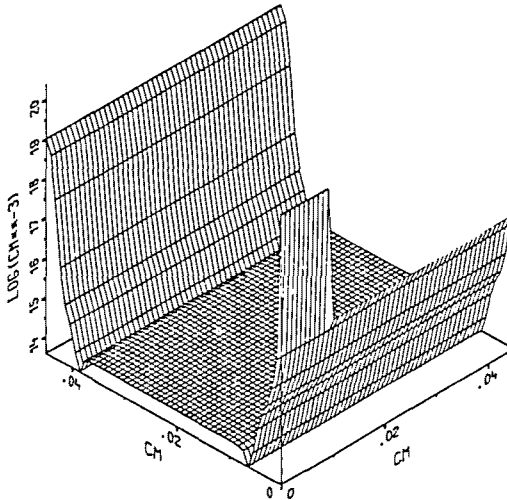


Fig 5: Doping concentration for the thyristor.

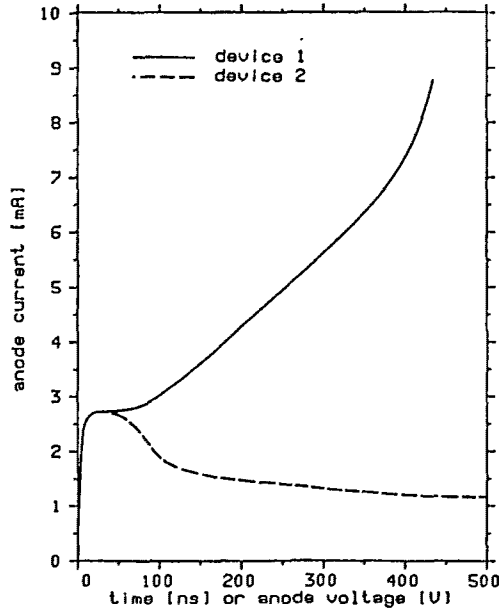


Fig 6: Transient anode current for $U_A = 1000V/\mu s \cdot t$.

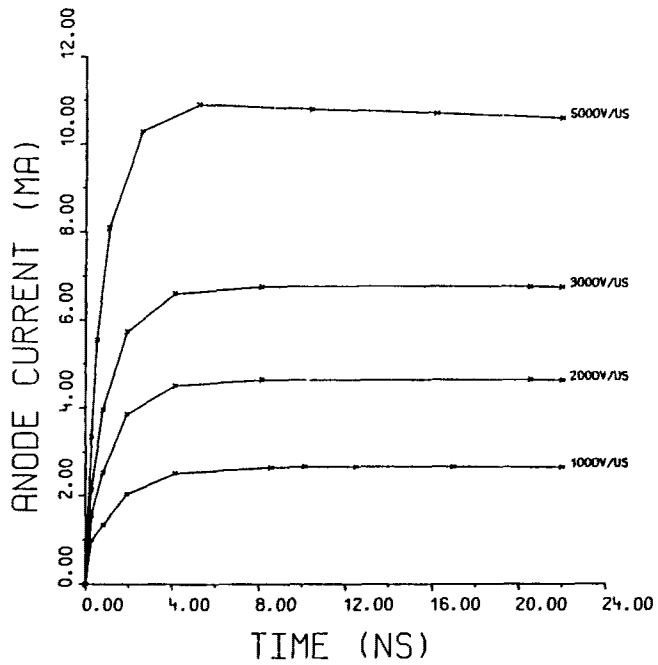


Fig 6a: Transient anode current for four different dU/dt ramps.

time characteristic for device 1 (solid line) and device 2 (dashed line). The initial phase of exponentially increasing current is identical for both devices. Then a constant current flow can be observed for about 50ns. This current loads the depletion capacitances. We have investigated the influence of different dU/dt ramps on this load current in view of linearity and numerical stability. The results are summarized in fig.6a (anode current versus time). The actual time steps which are automatically chosen by the program are marked with dots. The plot shows the theoretically expected linear dependence of the load current from the applied dU/dt . No difference between shorted and nonshorted devices has been noted during this time period but at about 50ns (which corresponds to an anode bias of 50V) the characteristics in fig.6 visually depart from each other. For device 1 we can first observe a linear increase of the anode current with a slope of about $15\text{mA}/\mu\text{s}$. This increase becomes exponential and leads to triggering at $t=450\text{ns}$ ($U_A = 450\text{V}$). The characteristic for device 2 has been calculated up to $t=1\mu\text{s}$, with a corresponding anode voltage of 1kV. The actual number of time steps TS, the maximum time step MAX, the minimum time step MIN, the number of grid updates GU and the final number of grid points GP are summarized in table 1.

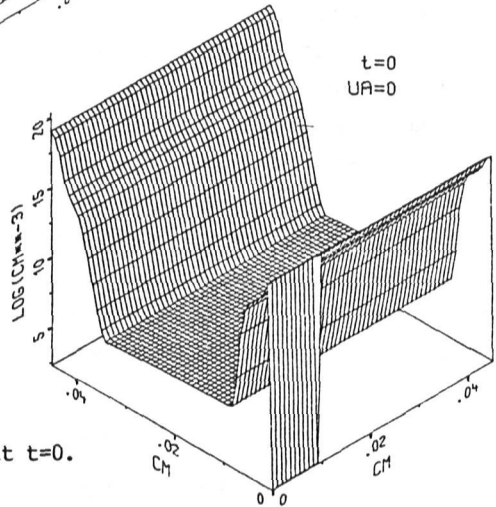
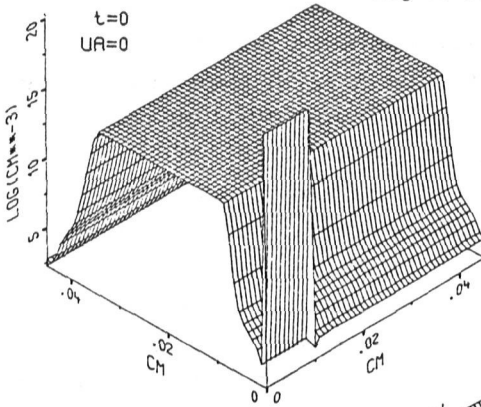
Table 1

Dynamically calculated program parameters

	TS	MAX	MIN	GU	GP
Device 1	30	124.8ns	0.28ns	6	1325
Device 2	21	282.7ns	0.28ns	4	1281

From this data it is evident that an accurate calculation of the triggered device 1 requires better control of the discretization and of the time steps.

In the following, we discuss snapshots of the electron and the hole concentration for both devices. Fig.7 and fig.8 show the electron and the hole concentration at $t=0.$, i.e. at equilibrium. The solution is certainly identical for device 1 and device 2.

Fig 7: Concentration of electrons at $t=0$.Fig 8: Concentration of holes at $t=0$.

The next series is taken at $t=25\text{ns}$ ($U_A=25\text{V}$) during the "load phase". Figs.9-12 show the electron and hole concentration for device 1 and device 2, respectively. We observe that the electron concentration in the pn-junction, which should block, is significantly higher for the unshorted device 1 in comparison to the same quantity for device 2. The hole injection from the anode is markedly higher for device 1 and the excess holes flood the bulk. For device 2, the hole concentration close to the blocking pn-junction is not affected at this time by the injected holes. However, the total current is identical at $t=25\text{ns}$ (see fig.6).

Fig 9: Concentration of electrons
for device 1 at $t=25\text{ns}$.

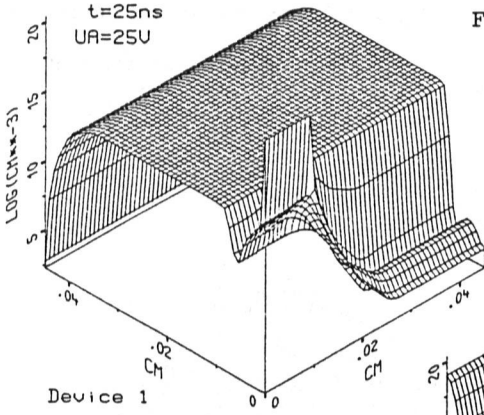


Fig 10: Concentration of holes
for device 1 at $t=25\text{ns}$.

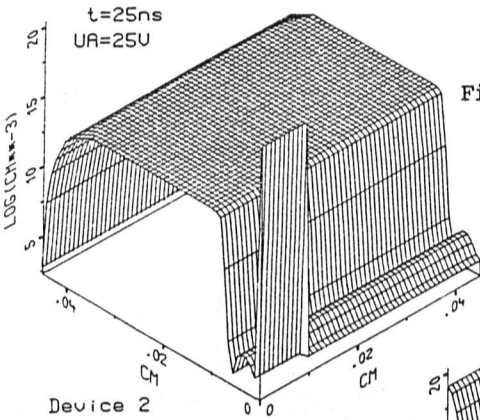
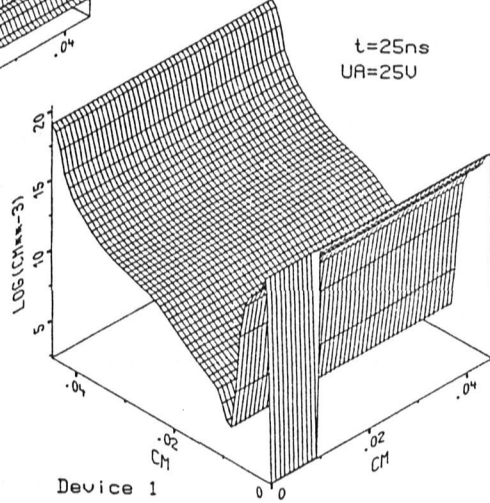


Fig 11: Concentration of electrons
for device 2 at $t=25\text{ns}$.

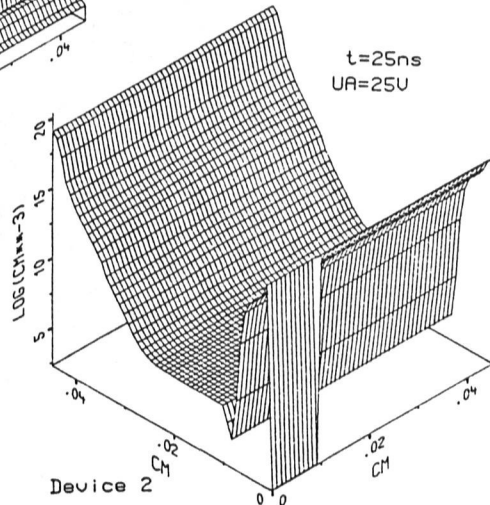


Fig 12: Concentration of holes
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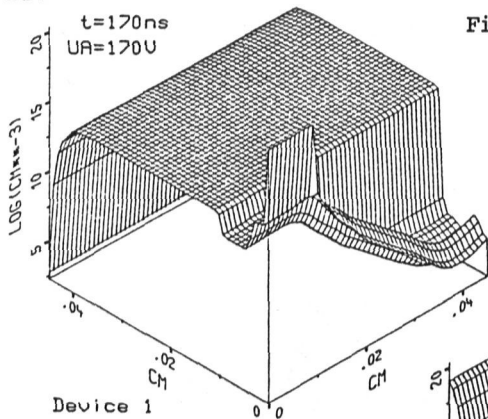


Fig 13: Concentration of electrons for device 1 at t=170ns.

Fig 14: Concentration of holes for device 1 at t=170ns.

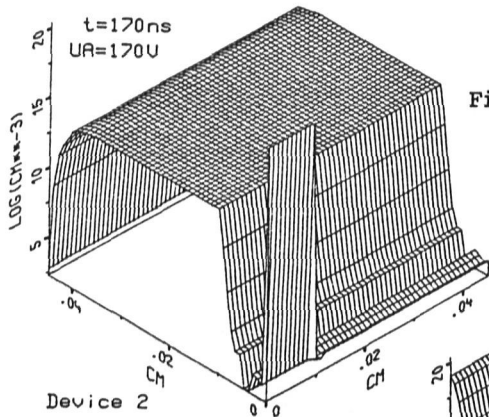
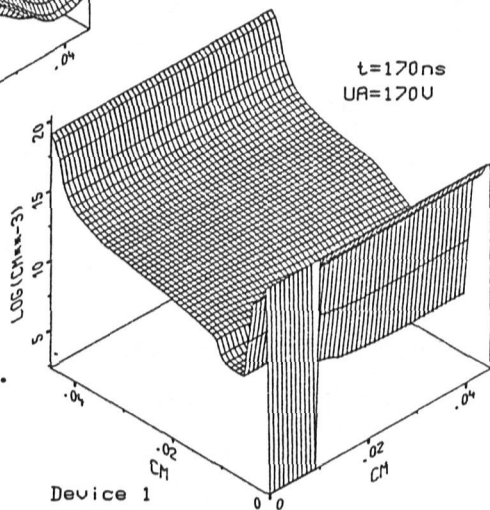


Fig 15: Concentration of electrons for device 2 at t=170ns.

Fig 16: Concentration of holes for device 2 at t=170ns.

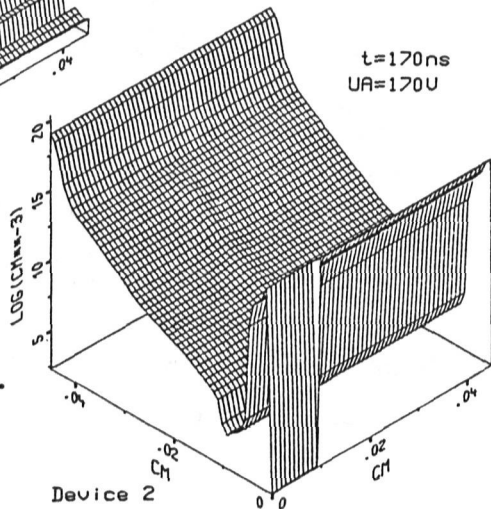


Fig 17: Concentration of electrons

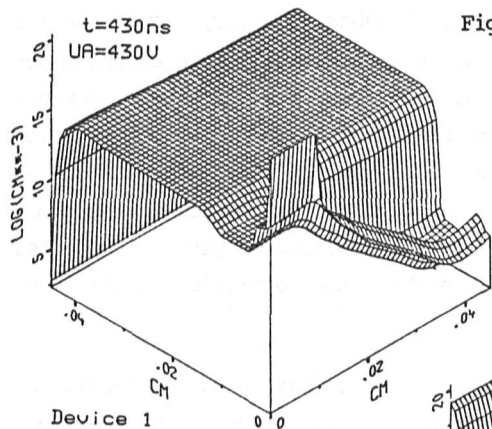
for device 1 at $t=430\text{ns}$.

Fig 18: Concentration of holes

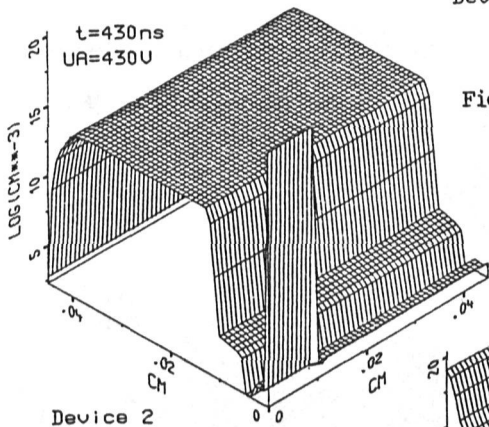
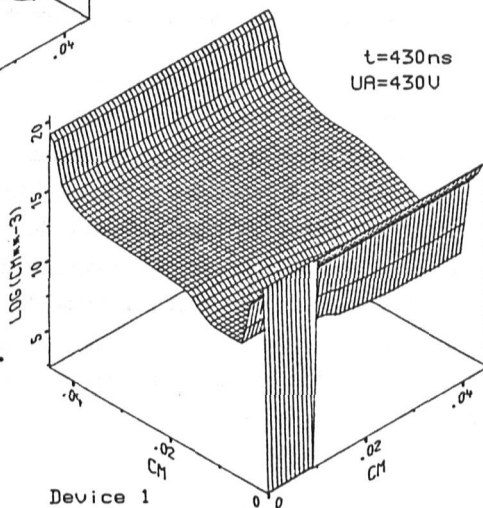
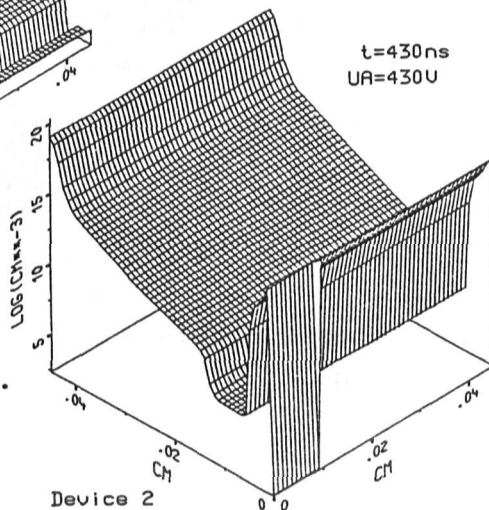
for device 1 at $t=430\text{ns}$.

Fig 20: Concentration of holes

for device 2 at $t=430\text{ns}$.

Fig 19: Concentration of electrons

for device 2 at $t=430\text{ns}$.

The next snapshot is taken at $t=170\text{ns}$ ($U_A=170\text{V}$). The electron concentration for device 1 (fig.13) shows a slightly more extended depletion region, but the level is already above the intrinsic concentration due to the injection from the emitter. The injection of holes (fig.14) from the anode is so strong now that the entire n-body is flooded. The electron concentration (fig.15) for device 2 has only insignificantly changed compared to the previous snapshot. The holes injected from the anode have reached the depletion region yet (fig.16).

The next series is taken close to the triggering of device 1 at $t=430\text{ns}$ ($U_A=430\text{V}$). The carrier concentrations in device 1 (figs.17,18) have reached enormously high values during this operating condition. There is almost no barrier left, particularly because of the hole concentration. In device 2, we can see the formation of a wide depletion region instead (figs.19,20). The level of the hole concentration due to injection from the anode did not characteristically increase compared to the distribution depicted in the previous snapshot (see fig.16).

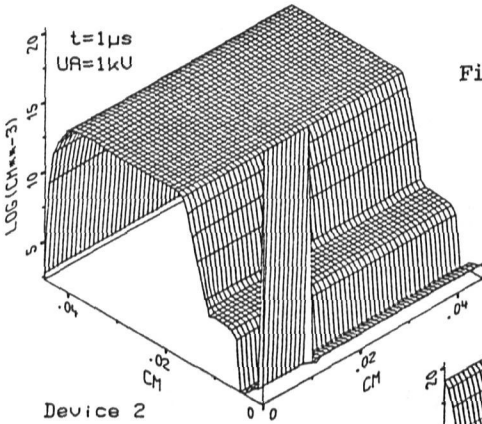
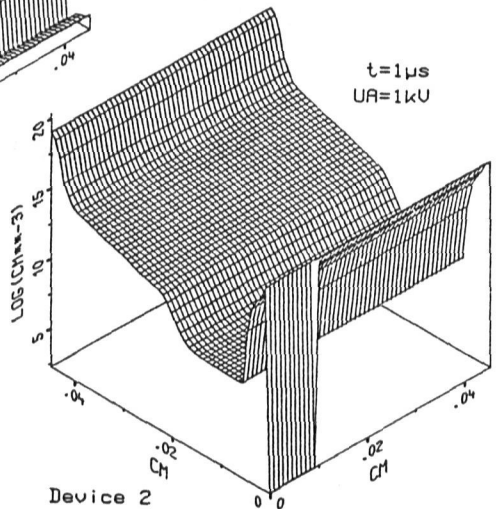


Fig 21: Concentration of electrons for device 2 at $t=1\mu\text{s}$.

Fig 22: Concentration of holes for device 2 at $t=1\mu\text{s}$.



It is clear that the final snapshot at $t=1\mu s$ is provided (figs.21,22) for device 2 only. One can easily observe the wide depletion region which is capable of blocking 1000V. The levels of the carrier concentrations there have increased as compared to the levels at $U_A=430V$, due to relatively strong thermal generation.

Conclusion

A novel 2-D transient simulation system BAMB I has been presented. Basically it has been designed for the analysis of power devices in view of the high voltage/high current operating points. Sophisticated algorithms for the spacial and time discretization have been designed and successfully applied. Thereby, the program system has become a more general software tool for semiconductor device simulation. As a demonstration, results of a study of the rate effect in power thyristors have been presented and analyzed.

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References

- /1/ O.Manck, W.L.Engl, "Two-Dimensional Computer Simulation for Switching a Bipolar Transistor Out of Saturation", IEEE Trans.Electron Devices, Vol.ED-22,pp.339-347,June 1975.
- /2/ M.S.Adler,V.A.K.Temple, "The Dynamics of the Thyristor Turn-On Process", IEEE Trans.Electron Devices, Vol.ED-27,pp.483-494, Feb.1980.
- /3/ V.C.Alwin et al, "Time-Dependent Carrier Flow in a Transistor Structure Under Nonisothermal Conditions", IEEE Trans.Electron Devices, Vol.ED-24,pp.1297-1304,Nov.1977.
- /4/ A.Nakagawa,D.H.Navon, "A Time-and Temperature-Dependent Simulation of the GTO Turn-Off Process", IEDM Techn. Digest 1982, pp.496-499.
- /5/ L.J.Turgeon, D.H.Navon, "Two-Dimensional Nonisothermal Carrier Flow in a Transistor Structure under Reactive Circuit Conditions", IEEE Trans.Electron Devices, Vol.ED-25,pp.837-843, July 1978.
- /6/ Y.Shimizu et al, "Numerical Analysis of Turn-Off Characteristics for a Gate Turn-Off Thyristor with a Shorted Anode Emitter", IEEE Trans.Electron Devices, Vol.ED-28,pp.1043-1047,Sept.1981.
- /7/ A.F.Franz et al, "Finite Boxes - A Generalization of the Finite-Difference Method Suitable for Semiconductor Device Simulation", IEEE Trans. Electron Devices, Vol.ED-30,pp.1070-1082,Sept.1983.
- /8/ G.D.Hachtel et al, "Semiconductor Analysis Using Finite Elements - Part II: IGFET and BJT Case Studies", IBM J.Res.Dev., Vol.25,pp.246-260,July 1981.
- /9/ G.Franz et al, "A Quasi Three Dimensional Semiconductor Device Simulation Using Cylindrical Coordinates", Proc.NASECODE III Conf.,pp.122-127,June 1983.