MODELLING OF LDMOSTS WITH ION-IMPLANTED AND SIPOS SURFACE LAYERS

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Abstract

The specific on-resistance of lateral DMOS transistors is calculated and compared for two types of device, the 'resurfed' structure and a surface implanted SIPOS covered structure. Device parameters are first chosen so as to give 600V breakdown for each type. It is shown that an LDMOS device with a surface implanted layer and SIPOS overlay gives superior performance with respect both to on-resistance and insensitivity of the breakdown voltage to fluctuations in substrate doping density.

Introduction

The 'Resurf' technique [1] has been applied to good effect in lateral DMOS transistors[2], in order to reduce the on-resistance-area product at any given design voltage. The disadvantages of the Resurf technique are the need for precise control of the charge in the epitaxial layer, and the sensitivity of breakdown voltage to the fluctuations in substrate doping density and epitaxial layer thickness-doping product.

An alternative method of reducing surface fields is to use resistive surface films such as SIPOS[3] between gate and drain to impose a linearly varying potential at the oxide surface. An additional advantage of this technique is the screening of electrostatically induced charge that

the resistive film gives.

In this work the calculations of avalanche breakdown voltage and drift-region resistance in the on-state are carried out for a conventional resurfed structure and a device with a surface implant and a SIPOS layer.

The latter will be shown to give a better combination of insensitivity to doping variations and low on-resistance.

2. LDMOS Structures

Figure 1 illustrates the resurfed LDMOS device with dimensions appropriate for 600 volt breakdown voltage. The epilayer thickness for this voltage is 18μm and the doping density is 6.5 x 10^{14} cm^{-3} which corresponds to 1.87 x 10^{-7} coul/cm^2 epilayer charge.

The alternative LDMOS structure with an ion-implanted surface region and SIPOS overlay, is shown in Figure 2, again with dimensions appropriate to 600 volts avalanche breakdown.

3. Breakdown voltage

The potential distribution is found by solving Poisson's equation

$$\nabla . \nabla \epsilon \phi = - \rho \qquad (1)$$

where ϕ is the electric potential, ρ is the volumetric charge density and ϵ is the permittivity. Equation (1) is solved in 2-dimensions by an off-state computer program SWANOFF2 [4] which is based on the finite element method. The programme uses quadrilateral, 8-noded isoparametric elements and allows for the automatic generation and optimisation of the mesh. The set of discretised non-linear algebraic equations are solved by a Newton-Raphson iteration scheme with an adjustable relaxation factor defined by a line search[5]. Frontal solution procedures are then used [6] to obtain the nodal potentials.

The mesh used to solve our two test problems consists of 1410 nodes and 439 elements. The boundary conditions are that V=0 at the source, gate and p substrate contacts, V = V_{app} at the

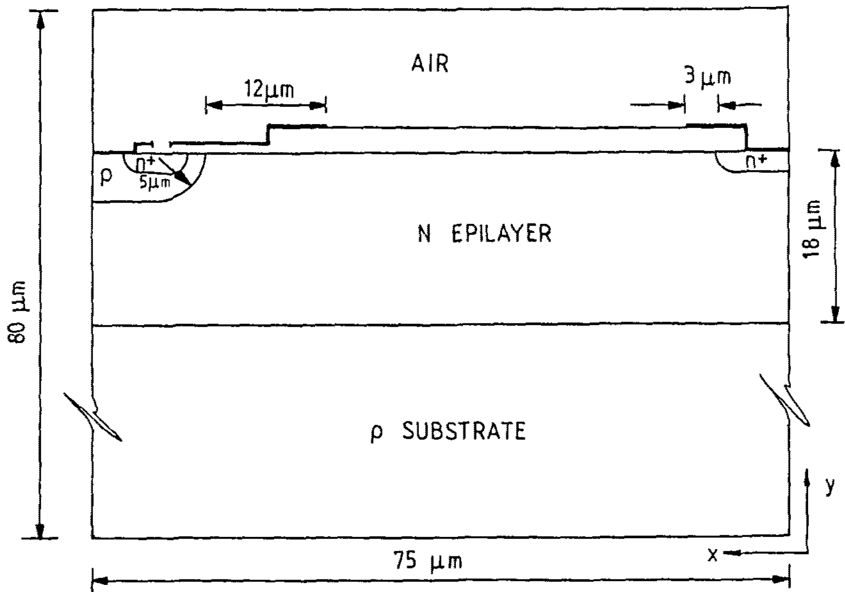

FIGURE 1: Geometry of a 600V Resurfed LDMOST.

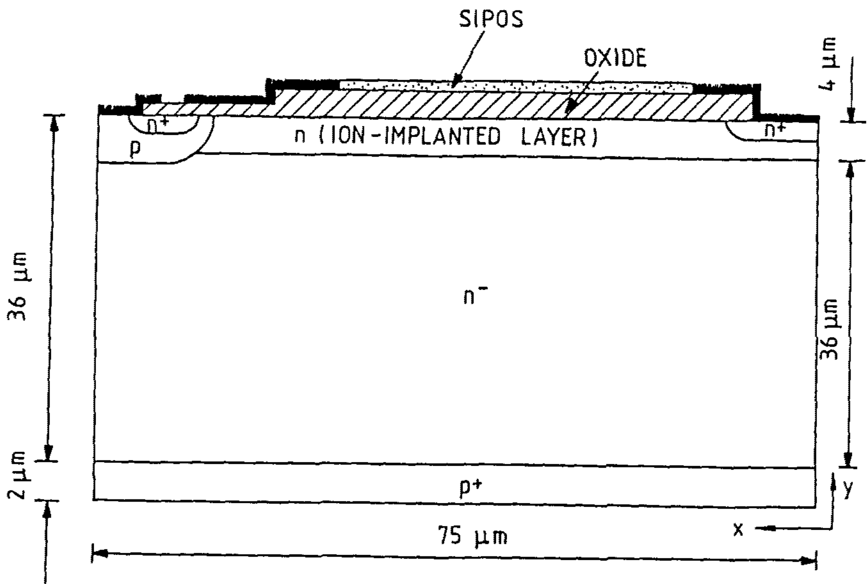

FIGURE 2: Geometry of a 600V Resurfed LDMOST with an Ion-Implanted layer and SIPOS overlay.

contact, and $\frac{\partial \phi}{\partial n} = 0$ at the axes of symmetry.

The device with a SIPOS layer, has an additional boundary condition where a linear potential distribution between the gate and drain is prescribed along the oxide surface [3,7].

The program has the facility of adjusting a particular material property (e.g. the doping density) iteratively in order to provide a solution at a prescribed breakdown voltage. Alternatively it can vary the applied voltage in order to determine the breakdown voltage for a specified set of device parameters. This results in an appreciable saving in run-time as the solution at one voltage can be used as the initialisation for the solution at the next voltage.

The breakdown voltage is evaluated by calculating the avalanche multiplication coefficients M_n and M_p for electrons and holes respectively along the field path passing through the maximum field point[8]. Other multiplication paths through different high field points are also checked. In each case a structure is obtained with a breakdown voltage of 600 volts by iterating as follows: For a given structure rough estimates of the doping densities of the epitaxial or the ion-implanted surface layer and the substrate for a given breakdown voltage in the bulk are used as a starting point. The multiplication coefficients M_n and M_p are then calculated. The doping density N_D and N_A are then adjusted in a direction such as to satisfy the condition that both M_n and M_p are both greater or equal to 2. The two previous solutions are used to interpolate or extrapolate the initialization of the next iteration. It should be noted that M_n and M_p should also be calculated for paths through other high field points in the device in order to ensure that breakdown occurs in the bulk.

An example of the results is shown in Figure 3 where the potential distribution and field density for the 600 volt LDMOST of Figure 1 are depicted. The effect of resurfing is quite clear since the depletion region extends towards the drain and breakdown occurs in the bulk. The effect of the ion-implanted and the SIPOS layers on the potential and field distributions for the 600 volts LDMOST of Figure 2 are shown in Figure 4. The uniformity of the electric field at the surface is evident.

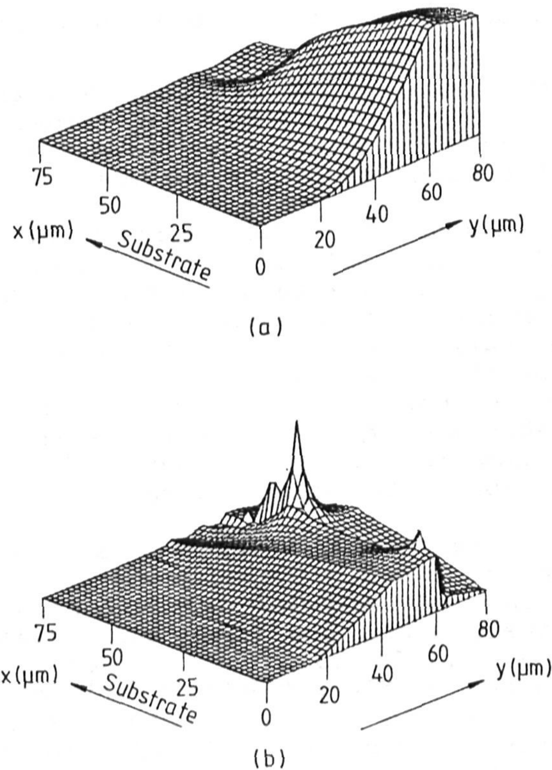

FIGURE 3: The Distribution of (a) Potential and (b) Electric Field for the 600V LDMOST of Figure 1.

4 On-Resistance

The on-resistance of the structures considered is calculated on the assumption that the dominant component is the resistance of the lightly doped extended-drain region. If the assumption of equipotential accumulation layers is made then conformal mapping may be used to calculate the resistance required.[9] The finite resistance of these layers may be taken into account by using very thin finite elements[10]. However the use of elements with very large aspect ratios may lead to ill-conditioning and unacceptably large round-off errors[6].

In our calculation of on-resistance a hybrid mesh was used, see Figure 5, consisting of 3-noded one-dimensional elements to represent the accumulation layer, and 8-noded quadrilateral two-dimensional elements to represent the n-region.

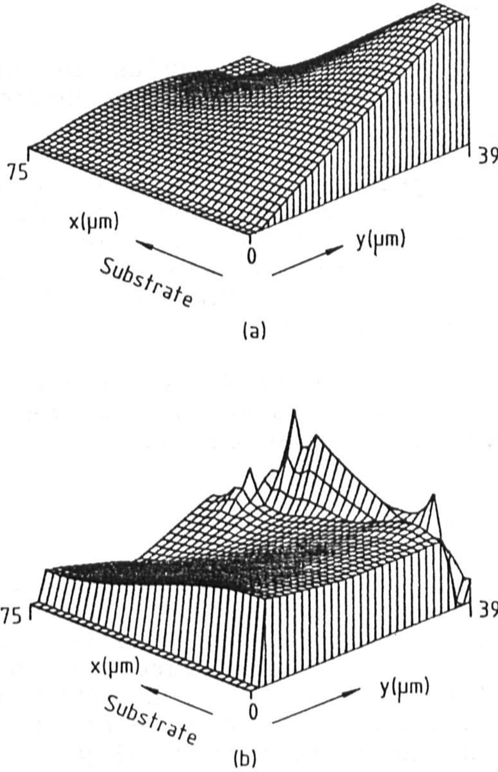

FIGURE 4: The Distribution of (a) Potential and (b) Electric Field for the 600V LDMOST of Figure 2.

FIGURE 5: Hybrid Mesh for On-Resistance Calculations

The solutions for the two devices under consideration were obtained using a mesh consisting of 215 elements and 687 nodes. The sheet resistance at a given position along the accumulation layer is a function of the potential at that position and this is taken into account in

the solution.

Figure 6 shows the results of on-resistance calculations for the Resurfed Structure (Device A of Fig. 1.).

The three graphs shown compare the calculations using conformal mapping, and the finite element solutions taking into account the voltage dependence of the accumulation layer sheet resistance (non-linear model) and assuming it constant (linear model)

Also shown in Figure 6 is the on-resistance of the surface implanted/SIPOS device having the same breakdown voltage. (Device B).

5 Discussion

Figure 7 shows how the breakdown voltage varies with substrate doping density for device (a) which is shown in Figure 1 and device (b) which is similar to the device in Figure 2 with a 2μm thick implanted layer but without a SIPOS overlay. The breakdown voltage of the conventional LDMOST (device a) drops sharply with slight variations in N_A, since breakdown can either occur under the gate metal edge with too much epilayer charge or at the drain diffusion with too little epilayer charge. Thus a similar variation of the breakdown voltage with the epilayer charge ($\approx t \times qN_D$) can occur. In contrast the device (b) is insensitive to variations of N_A when it is greater than approximately 3 x 10^{16} cm^{-3} since almost all the applied voltage is dropped in the n^-layer.

The SIPOS overlay helps to decrease the electric field at the surface and thus permits an increase in the ion-implanted layer doping density without degradation of the breakdown voltage. Hence a reduction of approximately 75% results in the on-resistance. This can possibly be still further improved for a fully optimised structure.

It is clear that such devices with ion-implanted surface layer and SIPOS overlays combine the advantages of higher yield because of the insensitivity to doping variation and low on-resistance, stability and reliability which the SIPOS film provides.

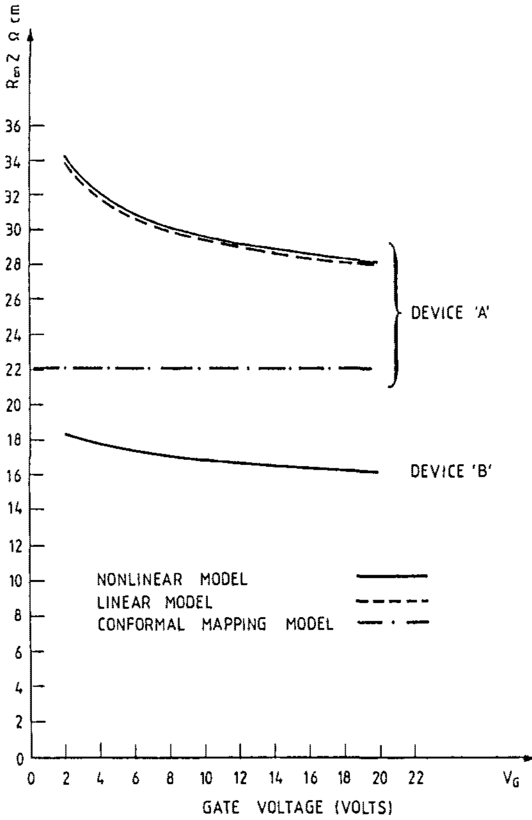

FIGURE 6: On-Resistance versus Gate Voltage for the LDMOST of Figure 1 (Device (a)) and for that of Figure 2 (Device (b))

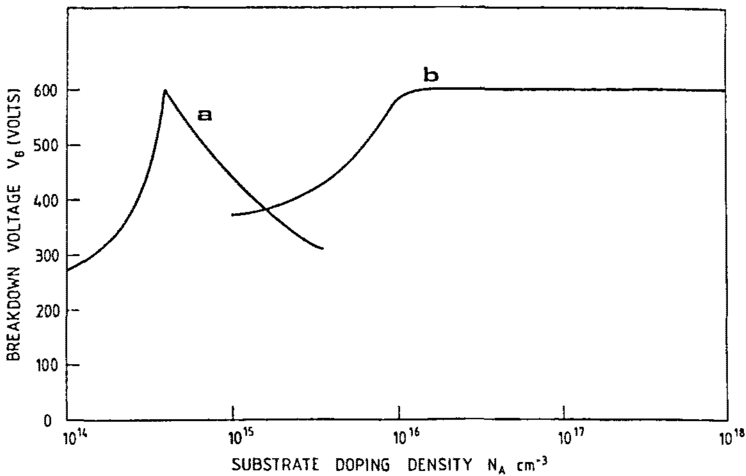

FIGURE 7: Breakdown Voltage versus Substrate Doping Density for Devices (a) and (b)

6 Conclusions

It has been shown that the sensitivity of the breakdown voltage in lateral DMOS resurfed devices to fluctuations in the epilayer thickness doping product may be substantially reduced by an alternative structure consisting of a surface implant and SIPOS overlay. The substantial improvement of the resurf structure over conventional LDMOS devices is not sacrificed in the alternative device proposed.

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