A 2/3D ANALYSIS OF THE THRESHOLD VERSUS PUNCHTHROUGH COMPROMISE IN VERTICAL DMOSTS

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ABSTRACT

2 and 3D numerical simulation (using the TRIPOS semiconductor analysis package) is used to study the effect of p-body profile tailoring on the threshold versus punchthrough compromise for vertical DMOSTS. A triple-implanted process, where compensation between n and p diffusions of comparable dose is used to give a composite profile with (relatively speaking) low peak and high tail concentrations, has been found to be of considerable value.

1. INTRODUCTION

Reduction of the threshold voltage for DMOSTs requires a lowering of the peak concentration of the p-body diffusion which, in turn, reduces the total p-body charge. The design of low threshold DMOSTs is complicated, therefore, by the need to avoid excessive depletion of this charge (and, hence, source-drain punchthrough, short-channel effects or parasitic bipolar turn-on) at high applied bias (1).

For many vertical DMOST structures, the problem is further compounded by the field peaks present at the unprotected corners given by triangular, square or hexagonal cell structures. Some field relief is provided by adjacent cells; thus, the gate track width can be expected to affect punchthrough resistance as well as breakdown potential (2).

Considerable alleviation of the resulting compromise between the threshold and punchthrough compromise between the threshold and punchthrough voltages can be obtained by appropriate tailoring of the p-body profile, for instance, through choice of an adequate channel-length via the n+ source and p-body junction depths or by implantation through a tapered polysilicon gate (3).

In the present work, 2 and 3D numerical simulation (using the TRIPOS package (2)) will be used to consider the implications of p-body profile modification via a triple-implanted process, where compensation between n and p diffusions of comparable dose is used to give a composite profile with, relatively speaking, low peak and high tail concentrations.

2. VERTICAL DMOS STRUCTURE

The schematic cross-section of an interdigitated vertical DMOST is shown in Figure 1 and the basic device parameters for a 200 v design outlined in Table 1.

The region between the n^+ source and the dotted line in Figure 1 represents, schematically, the modification to the reference DMOST structure introduced by the triple-implantation technology. The doping within this region remains p-type; the profile, however, is altered by compensation between the overlapping n and p implantations.

A typical comparison between the assumed lateral diffusion profiles for the conventional and triple-implanted structures is shown in Figure 2. For the conventional, single p-body implant, a dose of 2.10^{13} cm^{-2} produces a peak p-concentration almost immediately adjacent to the n^+ -p junction. In contrast, the composite, dual p-body implant with equal n and p doses of 5.10^{13} cm^{-2} produces produces an equivalent peak p concentration significantly displaced from the n^+ -p body junction and with a correspondingly much higher doping in the tails of the p- body distribution near the p - n^- junction.

For purposes of comparison, the triple-implanted composite profile shown in Figure 2 uses the same n^+ doping profile as that of the double-implanted structure. The peak concentration (and hence threshold voltage) is thus influenced by the diffusion parameters of all three (n^+,n,p) components. In practice, for a triple-implanted structure, the n^+ implant could be shallower, so that both the channel length and peak concentration would be determined primarily by the two compensating n and p components alone.

3. SIMULATION RESULTS

3.1 TRIPOS Input

The 1 - 3D semiconductor analysis package, TRIPOS, used for this study assumes both charge sheet and depletion approximations(2). Both approximations are entirely appropriate for the simulation of the breakdown and punch-through (off-state) characteristics of the device at high drain bias and the linear region (on-state) behaviour at low-drain bias.

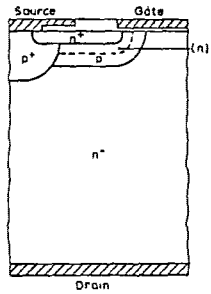

Fig 1 Schematic of triple-implanted DMOST

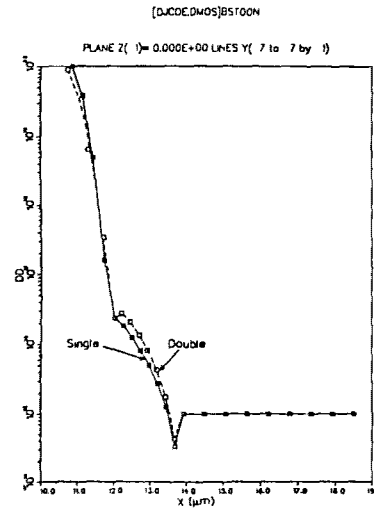

Fig 2 Lateral diffusion profile for single and dual p-body implant

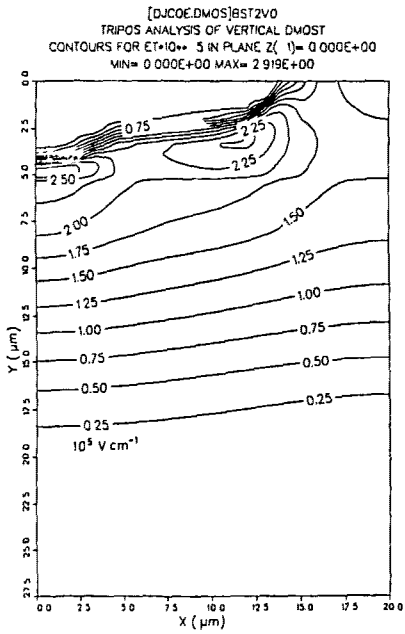

Fig. 3. Contours for total field

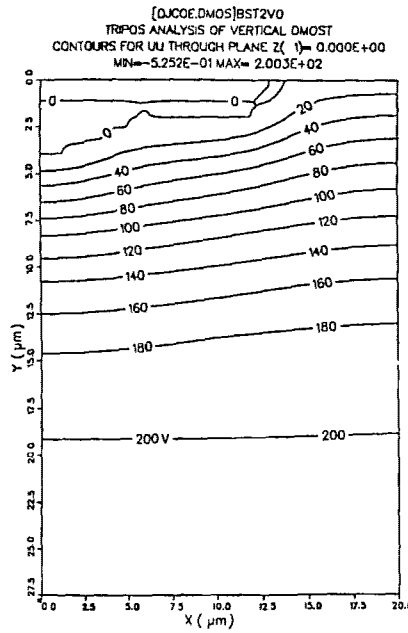

Fig 4. Contours for potential

Table 1

Basic DMOS device parameters

```
CONVENTIONAL DMOST (SINGLE P-BODY IMPLANT)
Select: Suprem2 or Gaussian vertical profile                    G
Select: Aligned or Offset squares or Interdigitated             I
Select: Tapered or Vertical polysilicon edge                    V
Select: N carriers Conductance Breakdown or Voltage             N
Is the guard (p+) diffusion omitted ?                           N
Give cell width in microns                                  37.0000
Give gate track width in microns                            15.0000
Give (p+) guard  window size in microns                      4.0000
Give contact window size in microns                          8.0000
Give source metallization track width                       14.0000
Give gate oxide thickness in microns                         0.1000
Give field oxide thickness in microns                        0.4000
Give (n+) source junction depth in microns                   1.1000
Give (n+) source lateral diffusion factor                    0.9330
Give (n+) source peak position in microns                    0.0000
Give (p ) body junction depth in microns                     3.5000
Give (p ) body lateral diffusion factor                      0.8100
Give (p ) body peak position in microns                      0.0000
Give (p+) guard junction depth in microns                    5.0000
Give (p+) guard lateral diffusion factor                     0.8750
Give (n-) epi thickness in microns                          23.5000
Give (n-) epi  signed  doping conc in cm**-3             1.0000E+15
Give (n+) source implantation dose in cm**-2             3.0000E+15
Give (p ) body   implantation dose in cm**-2             5.0000E+13
Give (p+) guard  implantation dose in cm**-2             3.0000E+15
Give signed oxide interface charge in cm**-2             0.0000E+00
Give gate  potential in volts                                5.0000
Give drain potential in volts                                0.0000
```

Table 2

TRIPOS input data file for basic DMOS free-carrier calculation

```
ALGORITHM 'CONVENTIONAL DMOST (SINGLE P-BODY IMPLANT)'
X( 1) =  0.00E+00
X( 2) =  5.00E-05
X(11) =  9.50E-04
X(14) =  1.10E-03
X(34) =  1.50E-03
X(41) =  1.65E-03
Y( 1) = -1.00E-04
Y( 2) = -2.00E-05
Y( 3) = -5.00E-05
Y( 5) = -2.00E-05
Y( 7) = -1.20E-05
Y(13) =  0.00E+00
Y(31) =  3.60E-04
Y(37) =  6.00E-04
Y(55) =  2.40E-03

REGION 'SOURCE CONTACT'
SURF=  X   1   8   Y   1   3
SURF=  X   1   5   Y   4  13
OR
VMIN=  0.00E+00

REGION 'DRAIN CONTACT'
SURF=  Y  55  55
DOPE=  1.00E+15
VMAX=  0.00E+00

REGION 'GATE CONTACT'
SURF=  X  15  41   Y   1   7
VMAX=  5.00E+00

REGION 'GATE OXIDE'
SURF=  Y   1  12
DOPE=  0.00E+00
EPSI=  3.90E+00

REGION 'SOURCE N+ DIFFUSION'
SURF= FUN3(-2.18E+17  1.30E+20  4.35E-05  4.35E-05 *
            2.20E-03  2.20E-03 -1.10E-03 -1.10E-03 )
DOPE= FUN3(-2.18E+17  1.30E+20  4.35E-05  4.35E-05 *
            2.20E-03  2.20E-03 -1.10E-03 -1.10E-03 )
EPSI=  3.17E+01
VMIN=  0.00E+00
VMAX=  0.00E+00

REGION 'DEEP P+ DIFFUSION'
SURF= FUN3(-1.00E+15  3.14E+19  1.58E-04  1.58E-04 *
            4.00E-04  4.00E-04 -2.00E-04 -2.00E-04 )
DOPE= FUN3( 1.00E+15 -2.14E+19  1.58E-04  1.58E-04 *
            4.00E-04  4.00E-04 -2.00E-04 -2.00E-04 )
EPSI=  3.17E+01
VMIN=  0.00E+00
VMAX=  0.00E+00

REGION 'P-BODY DIFFUSION'
SURF= FUN3(-1.00E+15  3.94E+17  1.43E-04  1.43E-04 *
            2.20E-03  2.20E-03 -1.10E-03 -1.10E-03 )
DOPE= FUN3( 1.00E+15 -3.94E+17  1.43E-04  1.43E-04 *
            2.20E-03  2.20E-03 -1.10E-03 -1.10E-03 )
EPSI=  3.17E+01
VMIN=  0.00E+00
VMAX=  0.00E+00

REGION 'N EPI'
DOPE=  1.00E+15
EPSI=  3.17E+01
VMIN=  0.00E+00
VMAX=  0.00E+00

SAVE CN
```

The input language for TRIPOS is designed for flexible specification of arbitrary device structures. A typical DMOS input file is shown in Table 2 and references a system-supplied Fortran function describing the various doping profiles via the superposition of a number of diffusions characterised by Gaussian distributions perpendicular to the device surface and by complementary error functions parallel to the surface.

This default function was sufficiently general to allow definition of a triple-implanted profile in both 2 and 3D. It was recognised, of course, that real device profiles might be rather different; facilities, however, are available within the TRIPOS package for the use of arbitrary user-specified functions or process-simulation files.

The breakdown and punchthrough simulations were carried out simply by submission of the input data file; the linear region calculations, however, were carried out in two stages (4). In the first stage, the free-carrier concentration (in either 2 or 3D) appropriate to a given gate potential was evaluated. With the DMOS turned on, a free-electron current path then existed between the source and drain contacts via the undepleted n^+ source, the inverted p-body channel and the undepleted n drift region. This electron distribution can be converted to a conductance profile though assumption of an appropriate function for field-dependent mobility and submitted to TRIPOS for a second stage simulation of the total device series conductivity (4);in these calculations, however, a constant mobility of 500 cm^2/vs was assumed.

3.2 2D Interdigitated DMOST

Typical equifield and equipotential contours for the reference DMOS are shown in Figures 3 and 4 respectively. The former clearly illustrates the field peak adjacent to the deep p^+ diffusion, which determines the breakdown potential for the device, and the somewhat lower field peak at the shallow p-body diffusion corner, which controls the degree of punchthrough.

For the assumed diffusion profile, punchthrough should occur first at the position of maximum field, some two-thirds around the p-body corner from the oxide-semiconductor interface. This will, therefore, be the critical region for parasitic bipolar turn-on,particularly under dynamic switching conditions. Under static conditions, however, the onset of punchthrough will be seen more clearly via channel-shortening along the oxide-semiconductor interface, which will manifest itself in non-saturation of the I_D-V_D transfer characteristic.

Such short-channel behaviour at high drain bias can be seen in Figure 5 where the channel potential is plotted

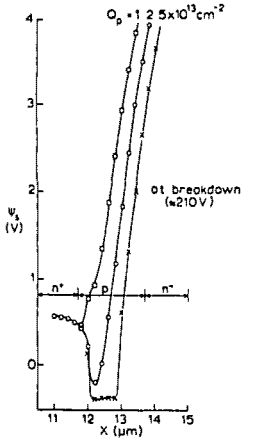

Fig 5. Channel potential v lateral position

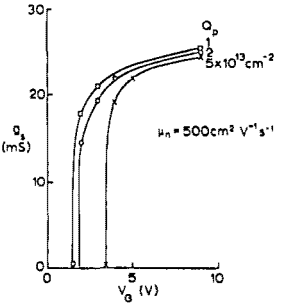

Fig 6. DMOST conductance v gate bias

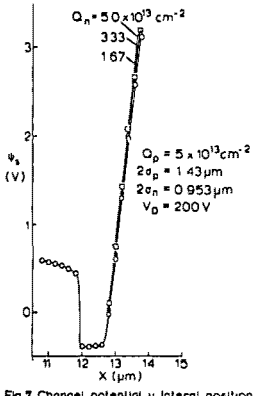

Fig 7 Channel potential v lateral position for triple-implanted DMOST

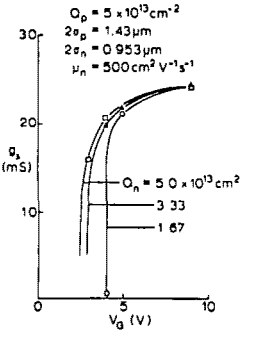

Fig 8 Conductance v gate bias for triple-implanted DMOST.

along the oxide-semiconductor interface for standard DMOSTs with various levels of p-body dose and diffusion coefficients adjusted to give a p n^- junction depth of 3.1 μm. In practice, the highest dose at 5.10^{13} cm^{-2} would give a well-saturated output characteristic, the middle dose of 2.10^{13} cm^{-2}, a marked shortchannel effect and the lowest dose, punch-through at well below the desired operating voltage of 200 V.

The corresponding linear region, turn-on characteristics of the device are shown in Figure 6. The chosen range of p-body implantation doses give device thresholds between 1.5 and 3.5 volts. A comparison between Figures 5 and 6 show clearly the trade-off between punchthrough and threshold voltages.

Figures 7 and 8 show equivalent simulated data for the triple-implanted DMOS. The composite p-body profile is made up of a high dose p-implant of 5.10^{13} cm^{-2} diffused to give a p n^- junction depth of 3.1 μm together with a range of n-implants of comparable dose but with two-thirds the diffusion coefficient.

For high applied drain bias, the variation of channel potential with lateral position given in Figure 7 shows essentially no change in the punchthrough performance despite increase of the compensating n dose from $1.67.10^{13}$ to 5.10^{13} cm^{-2}. These results confirm that little alteration to the tails of the p- profile has occurred.

In contrast, the linear region turn-on characteristics of Figure 8 show a progressive decrease in threshold voltage as the compensating n-dose is increased. Comparison of Figures 7 and 8 show that threshold voltages at least as low as 2V can be obtained without compromising the punchthrough performance of the DMOST.

3.3 3D Aligned-Square DMOST

The results of 3D TRIPOS simulations are included primarily to illustrate the extremely severe constraints placed on the compromise between punchthrough and threshold design interia through use of vertical DMOST cell geometries involving unprotected, acute-angled comers.

3D data for both potential and free-carrier distributions in the channel plane of the device are presented in Figures 9 and 10 respectively. For the convential structure, a single p-body dose of 2.10^{13} cm^{-2} is assumed; for the triple-implanted structure, a composite pbody profile with equal n and p doses of 5.10^{13} cm^{-2} and a 2/3 ratio between the n and p diffusion coefficients is taken. The view for each plot is taken looking towards the apex of the cell and, for clarity,

(a)
[DJCOE.DMOS]BST30V
SINGLE P-BODY IMPLANT FOR BST74
PLANE Y(7)= 1.667E-06

(b)
[DJCOE.DMOS]BST40V
DUAL P-BODY IMPLANT FOR BST74
PLANE Y(7)= 1.667E-06

V_{DS} = 200V
V_{GS} = 0V

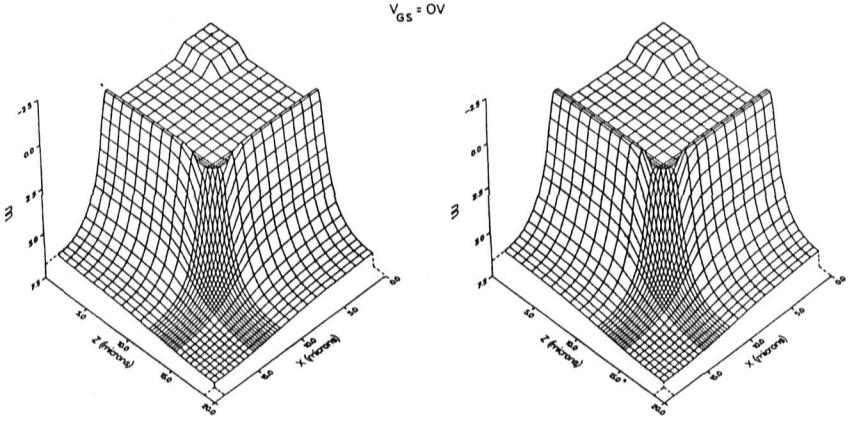

Fig. 9. Channel potential for a) Single and b) Dual p-body implant.

(a)
[DJCOE.DMOS]BST30N
SINGLE P-BODY IMPLANT FOR BST74
PLANE Y(7)= 1.667E-06

(b)
[DJCOE.DMOS]BST40N
DUAL P-BODY IMPLANT FOR BST74
PLANE Y(7)= 1.667E-06

V_{DS} = 0V
V_{GS} = 4V

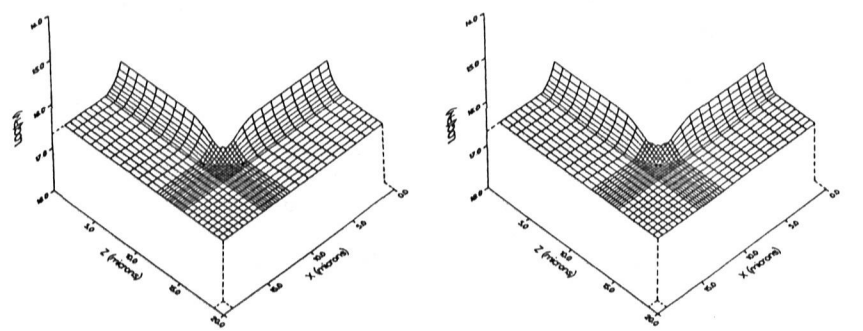

Fig.10. Free carrier density under gate for a)Single and b)Dual p-body implant.

the axes for both potential and free-carrier distributions are shown inverted. Off-state simulation with the drain biased near breakdown at 200V gives the comparative channel-plane potentials shown in Figures 9 a) and b). Along the edges of the square, these data are comparable with the 2D simulations of Figures 5 and 7, with the potential barrier separating the source and drain wider for the dual p-body implant than for the single p-body implant. At the corners, however, this potential barrier is removed entirely by the enhanced field and, for both structures, punchthrough currents will flow.

On-state simulation, with the drain biased low and the gate at 4 V gives the comparative channel-plane free-carrier distributions shown in Figure 10a and b). In both cases, a marked increase in free-carrier concentration is seen in the vicinity of the cell corner. In practice, current crowding will occur in this region and the effective threshold voltage of the device will be lowered considerably in comparison to a 2D interdigitated device.

Neither in respect of punchthrough nor in threshold has the use of p-body profile-tailoring proved of significant advantage at the critical corner regions of an aligned-square structure. It is clear, therefore, that without some form of corner field-relief, this type of device will prove extremely unsatisfactory.

There are, of course, a number of techniques for providing this field-relief. The most obvious solution is to increase the corner angle either through use of a hexagonal cell pattern or through bevelling or radiusing the corner. An alternative is to bury the corners in a deep p^+ diffusion, with further corner protection provided by extending these p^+ diffusions towards the cell interstices in the shape of continuous p^+ crosses(3).

4. CONCLUSIONS

The use of a triple-implanted process, where compensation between n and p diffusions of comparable dose is used to give a composite p-body profile with (relatively speaking) low peak and high tail concentrations, has been found to be particularly effective in improving the punch-through performance of low threshold vertical DMOSTs.

Such improvement, however, is not sufficient to prevent corner-enhanced punchthrough and threshold lowering for device structures with acute-angled (triangular or square) cell geometries. Since these problems occur in addition to those of premature breakdown, these corners should be protected by rounding or by burying in p^+ diffusions.

The numerical simulations were carried out for relatively deep diffused junctions. Although the results are equally relevant to technologies based on shallower junctions, the simultaneous use of both bevelled-gate and high energy implantation techniques provide a powerful means of p-body profile control which may give sufficient margin against field-enhanced corner effects.

6. REFERENCES

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(2) COE, D.J., WHIGHT, K.R., TREE, R.J. and VEVERIS, A.J. Proc. NASE CODE III, p 102, Galway, June 1983.

(3) TIHANYI, J., HUBER, P., STENGL, J. Proc. 1EDM, p 692, Washington, Dec. 1979

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