CONTROL OF WIDTH EFFECTS IN SMALL GEOMETRY CMOS DEVICES

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Process simulation is particularly appropriate to production control in CMOS IC fabrication. The process complexity and the divergent characteristics of the two transistor types make optimisation of their performance difficult. Simulation provides a fast route to test compromises in process specifications. However, if the process simulation package is to be useful in a production environment it must be available to the non-expert and the results must be suitable for use in a device model.

This paper presents a process simulation of small geometry (2µm) CMOS devices. Previous studies on narrow width effects in MOS transistors have concentrated on NMOS or N-well CMOS technologies. The present work concentrates specifically on width effects in a P-well CMOS process where diffusion of both the field implant and the P-well must be modelled during field oxidation. The simulation results allow the effective channel width of the MOS transistor to be determined.

1. INTRODUCTION

Process simulation is well established as a valuable tool in the semiconductor fabrication industry. SUPREM (1), has been the most widely used program to simulate impurity distribution in the vertical direction in the silicon wafer at each fabrication stage. As device geometries are shrunk for VLSI, one-dimensional simulations continue to be important but lateral effects in the silicon can no longer be ignored. Process simulations are now required in two and three dimensions in order to obtain an accurate description of the MOS transistor structure and its performance in an integrated circuit. Simulation programs are particularly useful in the case of CMOS technology where the fabrication process is both lengthy and complex. A two-dimensional simulator can be used in conjunction with SUPREM to simulate both length and width effects in the n-channel and p-channel MOS transistors of a bulk CMOS process. This paper is concerned with the prediction of the effective

width, W_{eff}, of the n-channel device in the P-well of a bulk CMOS process.

The problem of determining channel width in MOS devices has been treated by several authors. While ion implantation can be simulated relatively easily, any model of the impurity redistribution which takes place during field oxidation is complicated by the moving silicon-silicon dioxide interface. In SUPRA (3), Chin et al. use analytical models for diffusion during the high temperature field oxidation step. When a numerical approach is taken, the most common method has been to apply a time-dependent co-ordinate transformation so that the simulation area in the transformed system is rectangular and stationary. Authors who have implemented this method include Penumalli (4) and Tielert (5,6) who use a finite difference discretisation in their programs BICEPS and LADIS respectively. Maldonado et al (7) use the method of lines in ROMANS II. Seidl (8) uses a finite difference discretisation coupled with a multigrid method. Salsburg et al (9) use the finite element method in FEDSS, however impurity segregation effects at the moving silicon-silicon dioxide interface are neglected. While Maldonado has presented results of the simulation of transistor width effects in an N-well CMOS process, other authors have tended to restrict their attention to NMOS technology.

In these cases a uniform rectangular network of grid points is adequate for the finite difference method in modelling the diffusion of the field implant during oxidation. However, this approach is not possible in the case of a P-well CMOS process because the mesh must accommodate not only the channel stop region under the field oxide, but also the extent of the P-well in the vertical direction as shown in figure 1. To avoid an inefficient mesh structure, the program uses a non-uniform rectangular grid which comprises a fine mesh at the silicon surface to cover the field implant, and a coarse mesh throughout the rest of the P-well where impurity concentration varies less rapidly. The present paper is concerned with the finite difference method but the flexibility of a finite element method would also be useful in this case.

2. MODELLING CHANNEL WIDTH EFFECTS IN THE P-WELL OF A CMOS PROCESS

Simulation of the P-well formation up to the point in the process where the wafer receives the field implant of boron is well simulated in one-dimension by SUPREM (1), and, since this program is discussed extensively in the literature no discus-

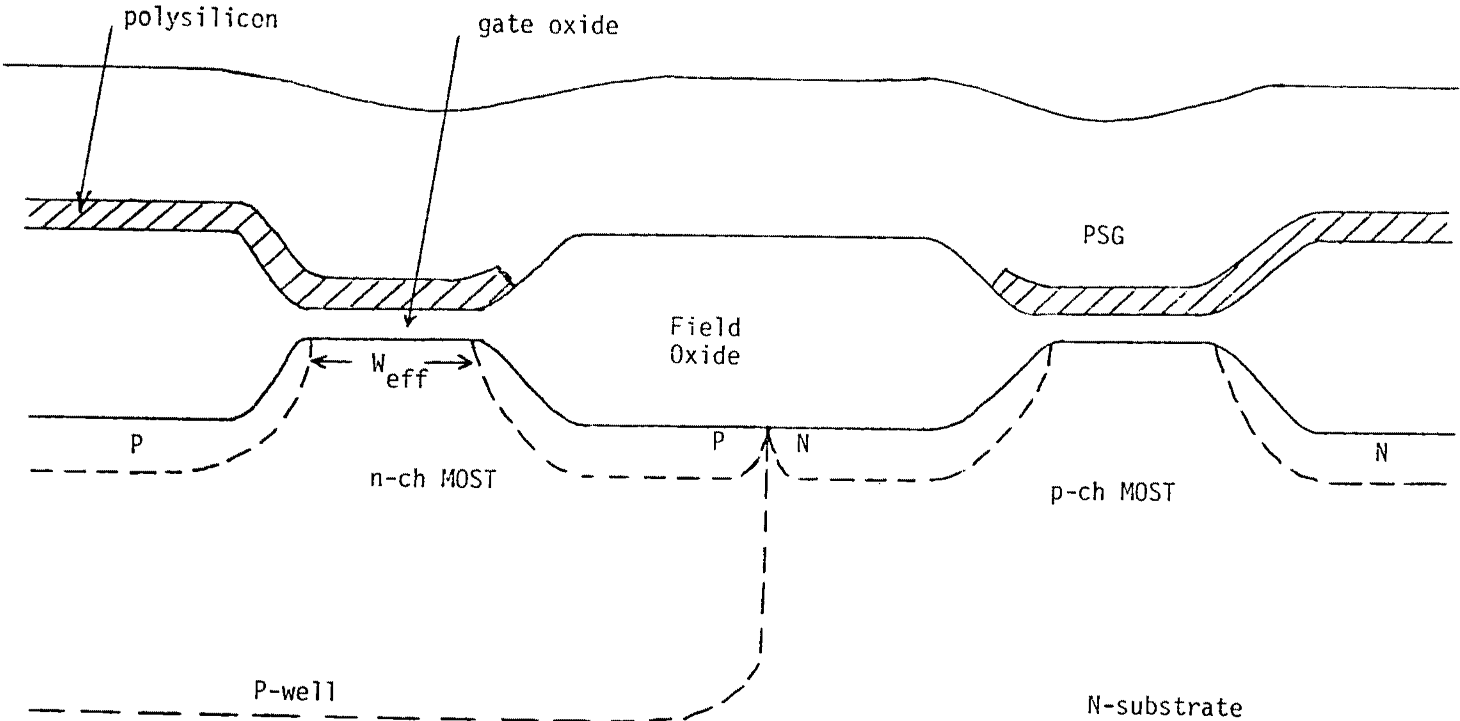

Figure 1 : A typical bulk P-well CMOS structure (for clarity, contact windows and metal have been omitted.)

sion is necessary here. Initial processing includes an N-substrate implant of phosphorus and a P-well implant of boron with subsequent drive-in. Boron is implanted into the channel-stop region, and the nitride mask protects the active device region. Ion implantation models are well established (2). Figure 2 shows a contour plot of the impurity profile, where the real simulation area has been mirrored in order that the full transistor width be shown.

Field oxidation is modelled using the approach of Penumalli (4) with the use of a non-uniform rectangular grid. The process models are essentially the same as those used in SUPREM II, but extended to 2-D. A constant diffusion coefficient D is assumed, which is a good approximation for low concentration diffusion. The diffusion process is modelled by Fick's law /1/, subject to appropriate boundary conditions /2/.

$$\frac{\partial C}{\partial t} = D\nabla^2 C \qquad /1/$$

$$\left.\begin{aligned} C\left(\frac{k}{\alpha} - 1\right)v_n &= D\frac{\partial C}{\partial n} \quad ; \quad x = X(y,t) \\ C &= Csub \quad ; \quad x = x_m + X(y,t) \\ \frac{\partial C}{\partial y} &= 0 \quad ; \quad y = o \\ \frac{\partial C}{\partial y} &= 0 \quad ; \quad y = y_m. \end{aligned}\right\} \qquad /2/$$

C is the impurity concentration, t is time, X(y,t) is the position of $Si\text{-}SiO_2$ interface, k is the segregation coefficient, α is the amount of silicon consumed to produce one unit of silicon dioxide, v_n is the normal velocity of the $Si\text{-}SiO_2$ interface and C_{sub} is the substrate concentration.

A co-ordinate transformation is applied to convert the simulation area to a rectangle which is more suitable for the application of finite difference methods. An explicit difference scheme has been used, however small time steps are required to ensure numerical stability. Larger time steps can be

silicon dioxide

silicon nitride

-4 -2 0 2 4 microns y

0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 microns x

2E16

1E18
7E17
3E17
1E17
3E16
2E16

Boron implant
dose: 1.1E13 cm^{-2}
energy: 35keV

Concentration contours in cm^{-3}

2E16

P-well

1.5E16

Figure 2: Contour plot of doping profile after the field implant.

used in the Crank-Nicolson method to obtain a system of linear equations which is solved using the Gauss-Seidl iterative method. Boundary conditions are accommodated using virtual nodes outside the simulation area. Central differences are used for the diffusive terms and upwind differences for the advective terms. Figure 3 shows a typical non-uniform grid used by the program in the transformed (ζ,η) plane. Further processing steps which affect the distribution of dopants in the silicon consist of a neutral ambient drive-in for 500 mins at 1025°C, field oxide growth for 1100 mins at 900°C and an anneal for 30 mins at 1000°C. Figure 4 shows the net acceptor concentration in the first few microns of the P-well at the end of the fabrication process.

3. DISCUSSION OF SIMULATION RESULTS

A simulation of field oxide growth and impurity redistribution allows the effective channel width of the MOS transistor to be determined. If the encroachment of the field implant into the active device region under the nitride mask is W, and the original nitride track width is W_N, then the effective channel width W_{eff} is given by

$$W_{eff} = W_N - 2\Delta W \qquad /3/$$

Ideally the process simulation results should in turn be fed to a device simulator (1), but approximate dimensions of the channel width can be extracted from the impurity profile for initial process engineering purposes. From figure 4, ΔW = 0.75µm, W_N = 4µm so that W_{eff} = 2.5µm. This example illustrates an important consideration for optimisation of the width of the -channel MOS transistor. Because the segregation of boron into the field oxide during oxidation is so severe, an inert drive-in of the boron field implant is required to ensure that the impurity concentration at the silicon surface is sufficiently high at the end of the process. While the profile is driven in vertically, it also extends further into the active device region. By assuming a tolerance in W_N, the worst and best cases of W_{eff} can be determined. Knowledge of these device limits reduces the number of fabricate-test iterations and allows reliable CMOS integrated circuits to be designed.

Whilst this paper has dealt with the particular case of a P-well CMOS structure, the model can equally well be applied to nMOS, N-well CMOS and twin-tub CMOS technologies. Future extensions iNclude the incorporation of the concentration-

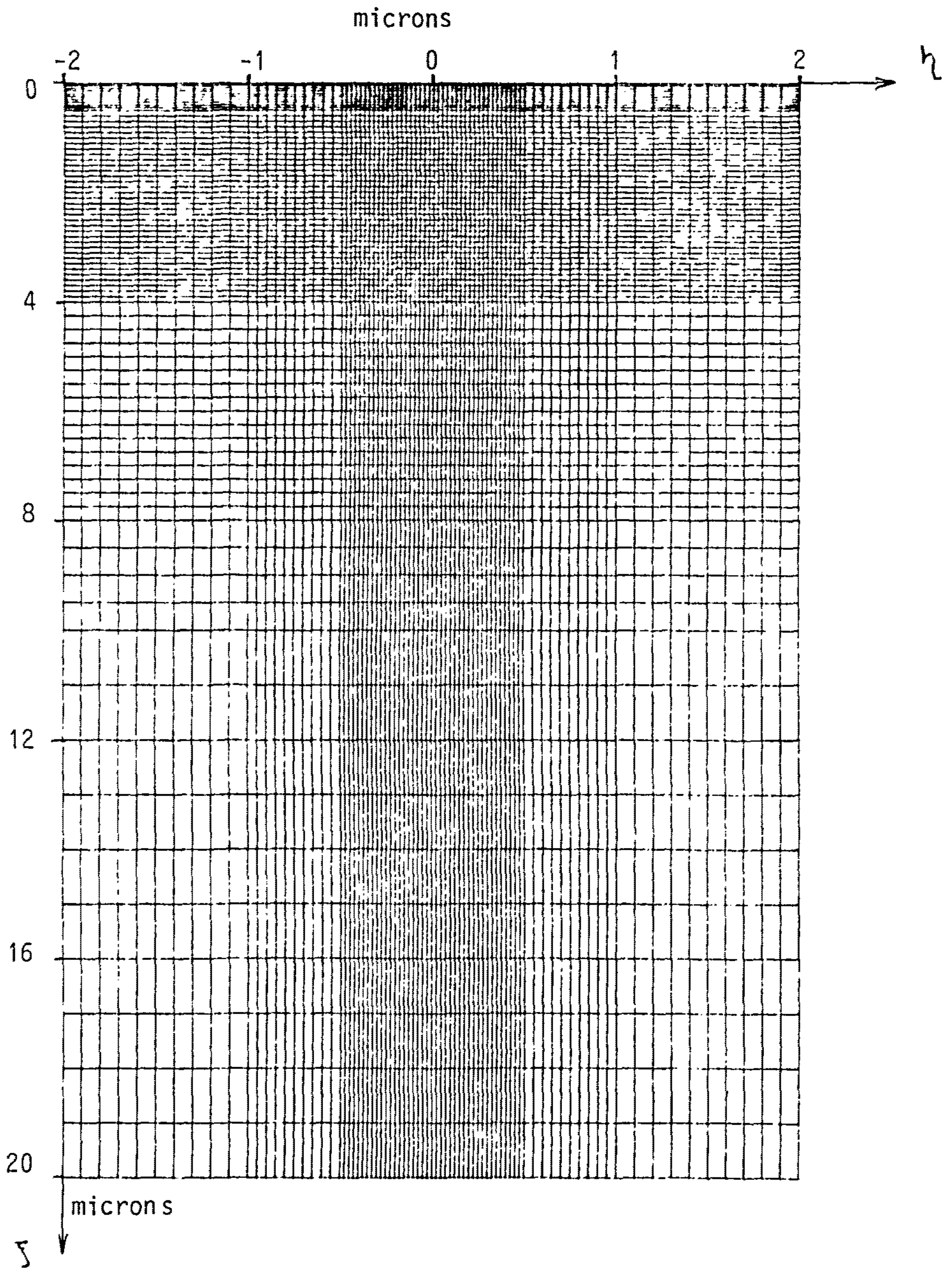

Figure 3: Non-uniform grid for finite difference method.

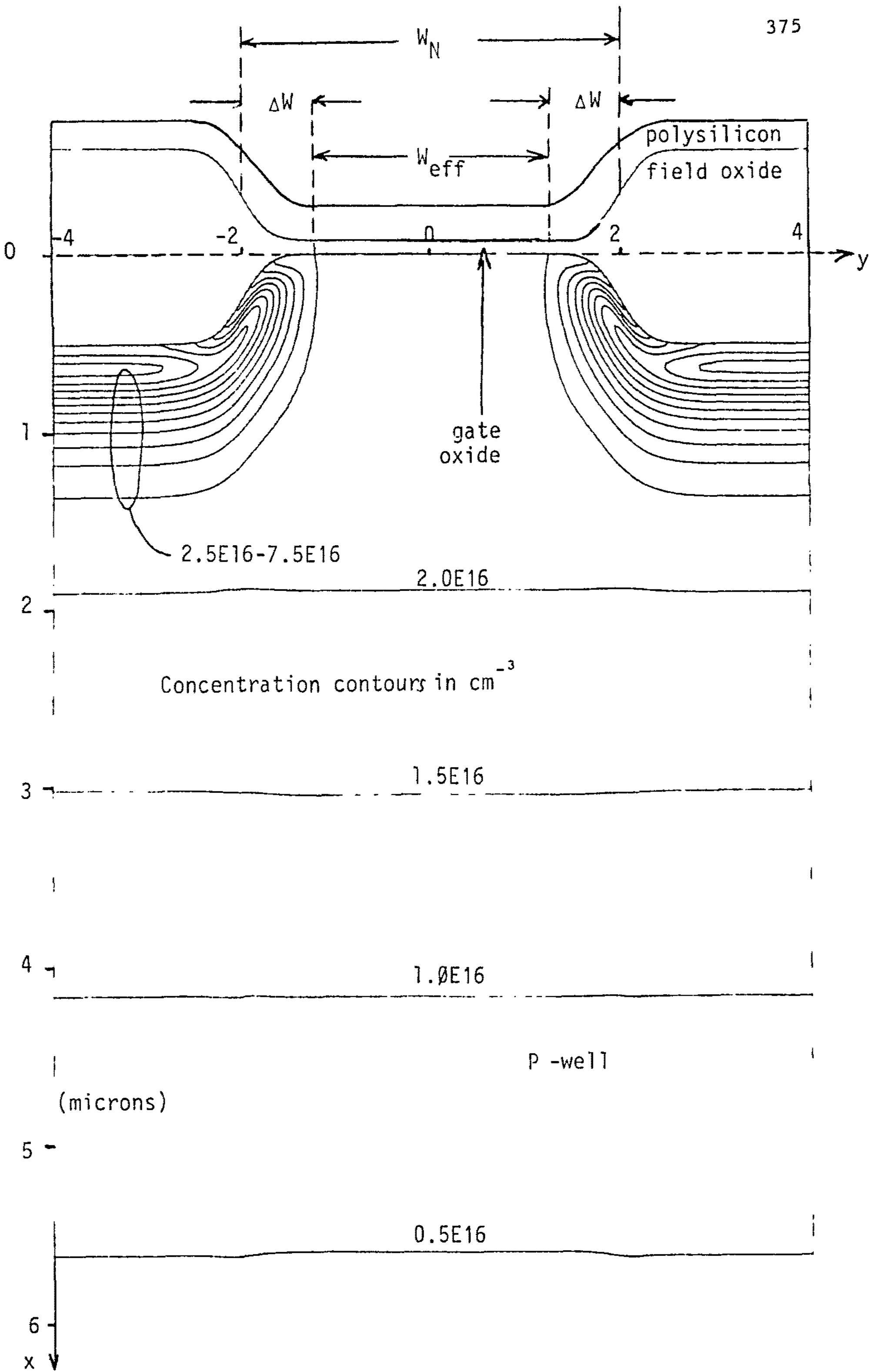

Figure 4: Contour plot of doping profile at the end of the fabrication process.

dependent diffusion coefficient D, and also the simulation of fully-recessed field oxide structures.

4. ACKNOWLEDGEMENTS

This work is part of a CASE project between Edinburgh University and Motorola Ltd,. East Kilbride. The authors wish to thank J. Burnie of Motorola for many helpful discussions.

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