A New Technique for Investigating Transient Latchup in CMOS Dynamic Circuits

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Abstract

A new technique has been developed to examine the effect of transient latchup-like behavior on CMOS dynamic circuits. Two-dimensional device simulations have shown that injected minority carriers can be rapidly collected at storage nodes and hence alter the logic state of a circuit. The effect of different structural components on this transient parasitic effect will be presented.

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Extended Abstract

Latchup holding voltage is a widely used parameter to define a latchup-free condition, because the device will not sustain latchup if the power supply voltage is below the holding voltage. This is true for static device operation, but it is not clear that transient current pulses due to the short turn-on delay time of the vertical p-n-p bipolar transistor in epi CMOS will not upset dynamic circuit operation due to injected minority carriers being collected by nearby circuit nodes [1]. In this work, a new technique for investigating the effect of transient latchup in CMOS dynamic circuits is developed, and two structures' dynamic latchup immunity in epi CMOS is investigated.

To investigate the transient effect due to latchup in the CMOS dynamic circuits, a capacitor or a diode is added to the pnpn latchup structure. The test structure using a capacitor and a 3.6 μm n^+ - p^+ spacing is shown in Fig. 1. The two dimensional transient device simulation was carried out using PISCES II. The 3V power supply voltage was lower than the latchup holding voltage (5 V). The transient latchup was triggered by injecting current from the forward biasing of the p^+-n well junction. The current was turned off after a short period of time ($<$ 5 nsec), after which the device returned to the normal blocking state and did not sustain the latchup. Charge was collected in the nearby capacitor due to the transient triggering, provided the triggering lasted longer than 0.4 nsec. This charge can alter the state of the dynamic circuit, and thus a transient latchup pulse can damage a circuit that is latchup free in static operation.

Two structures were investigated to determine factors which affect the transient latchup. One structure was a conventional retrograde n-well in an epitaxial substrate [2]. The second structure included a high dose p^+ implantation along the edge of the n-well. The addition of this implant improves the holding voltage, because the p^+ sidewall of the n-well acts as a block to the current flow, which decouples the lateral n-p-n transistor; therefore, the holding voltage increases with increasing implantation window width (Fig. 2). This structure also shows less sensitivity to the triggering current, since it takes a longer time to turn on both parasitic bipolar transistors as compared to the same structure without the implant. The charge collected by the capacitor due to the minority carriers flowing into the capacitor is plotted in Fig. 3. The collection of this charge alters the logic state of the capacitor in less than a nano-second which is six orders of magnitude faster than the milliseconds typically required to collect that much charge due to generation current. The structure with the n-well sidewall implant shows improved transient latchup immunity compared to the structure without the implant. The 2-D current flow in the structure with the implant shows that most of the current flows into the heavily doped bulk substate rather than into the n^+ node; therefore, most of the minority carriers are prevented from flowing into the capacitor. The same effect is also observed in the diode case. Here the reversed junction leakage current increases rapidly as latchup triggering continues, as shown in Fig. 4. This current can discharge a gate capacitor much faster than typical leakage currents. Other simulations will be presented demonstrating the effects of different structural components on transient latchup immunity.

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[1] W.-H. Chang, and M. D. Rodriguez, IEEE Elec. Dev. Lett. EDL-8, No. 6, 1987.

[2] D. Sharma, S. Goodwin-Johannson, D.S. Wen, C.K. Kim and C.M. Osburn, Proc. of 1st Inter. Symp. on ULSI, the Electrochem Soc., 1987.

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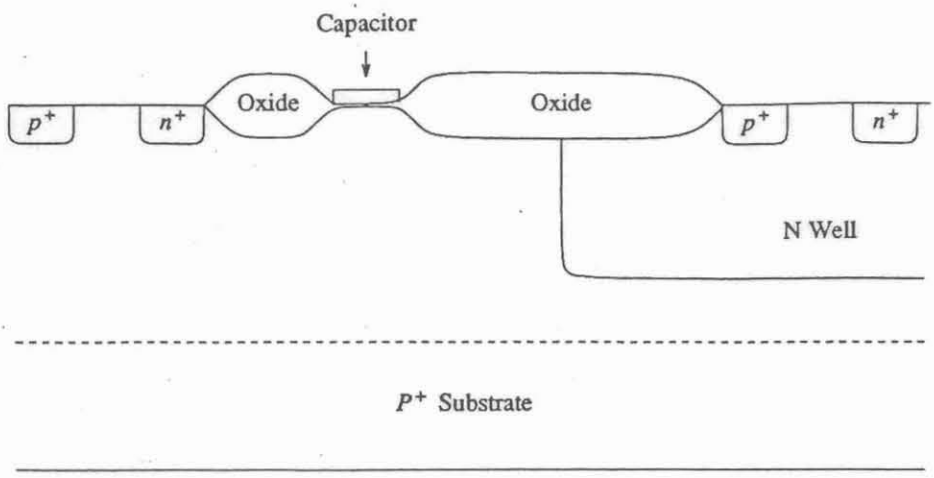

Fig. 1 The test structure using a capacitor and a total 3.6 μm n^+–p^+ spacing for two dimensional device simulation. The epi thickness is 3.5 μm. In the diode case, the capacitor is replaced by an n^+-p diode.

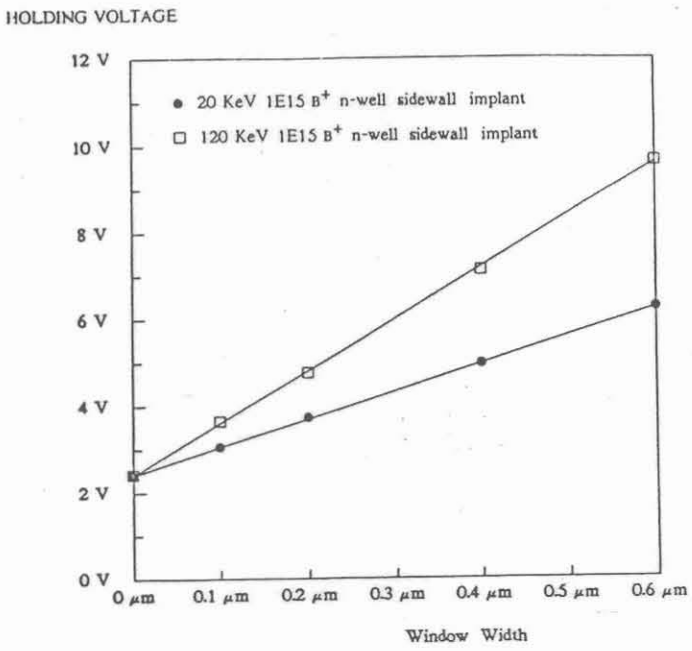

Fig. 2 The holding voltages vs. field implantation window width for two different implantation energy.

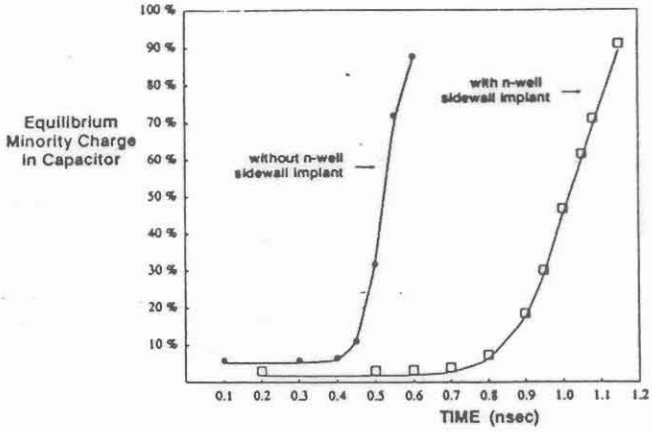

Fig. 3 The minority charge collected by the capacitor due to transient latchup triggering vs. the sustaining time of triggering current, where 100% of equilibrium minority charge corresponds to the charge in the inversion layer in equilibrium with the same bias.

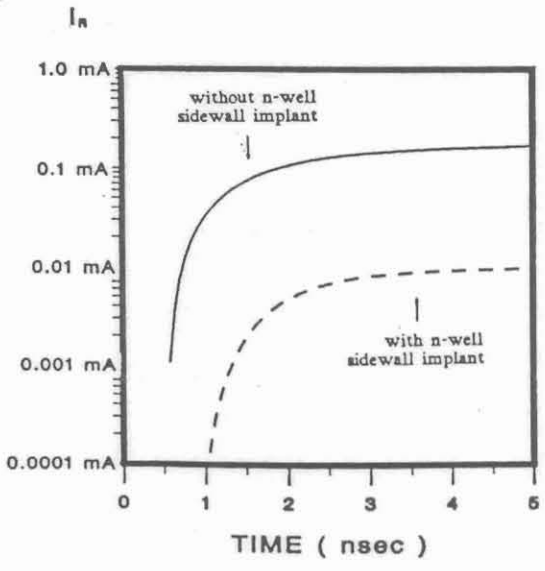

Fig. 4 The n^+-p diode leakage current during the transient.