TWO-DIMENSIONAL EMITTER-BASE JUNCTION CAPACITANCE FOR BIPOLAR TRANSISTOR CIRCUIT SIMULATION

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Abstract--A two-dimensional comprehensive quasi-static capacitance model for the emitter-base space-charge region of bipolar transistors is developed. The model includes the effects of emitter crowding, the geometry of the transistor, and the ohmic drop in the quasi-neutral base region. The present model is implemented in SPICE circuit simulator, and good agreement is obtained when the resulting transient response is compared with that obtained from a two-dimensional device simulator PISCES.

SUMMARY

The space-charge-region capacitance plays significant role in switching speed and frequency response of semiconductor devices, particularly for VLSI bipolar transistors because they have thin base regions which necessarily increases the base doping concentration, and thus decreases relative importance of the quasi-neutral base capacitance. Further, because of the small geometry of VLSI devices, two-dimensional effects such as emitter current-crowding and base resistance are important, and the extrinsic space-charge-region capacitance needs to be modeled appropriately. Most the previous treatments of the space-charge-region capacitance focus on the intrinsic region (or the planar region) [1]-[5]. Roulston and Kumar [6] developed an analytical model for the peripheral emitter-base space-charge-region capacitance, but the model is only valid for junctions under zero bias. Thus a two-dimensional comprehensive capacitance model is needed.

The purpose of the paper is to develop a comprehensive two-dimensional (planar and peripheral) quasi-static capacitance model for the emitter-base space-charge region of bipolar junction transistors. This capacitance model also applies to the space-charge-region capacitance of p/n junction diodes. The model includes the effects of the ohmic drop in the quasi-neutral base and describes the capacitance for all voltages and applies for practical junction profiles.

First, by dividing the device structure into three regions, the study focuses on the resistance and the geometry of the base region, from which a model for calculating the emitter-base junction voltage V can be found. A simple iterative technique is used to calculate V numerically. On the basis of the junction-voltage model and a recently developed one-dimensional capacitance model [4], we derive the planar and peripheral capacitances of the space-charge region. The present model is then implemented in SPICE circuit simulator, which uses a 1-D junction capacitance model, to assess the impacts of the present model on the transient and frequency responses of bipolar integrated circuits. Figure 1 illustrates the transient responses obtained from unmodified SPICE, from SPICE implemented with the present 2-D model, and from a 2-D device simulator PISCES for an inverter circuit with a fast input pulse.

Thus, it is anticipated that the study will aid more understanding on device behaviors and the present model can provide better accuracy than that of one-dimensional capacitance models for bipolar integrated circuit simulation.

REFERENCES

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FIGURE CAPTIONS

Fig. 1 Comparison of the transient responses simulated from unmodified SPICE, from SPICE implemented with the present 2-D model, and from a 2-D device simulator PISCES for the inserted inverter circuit.

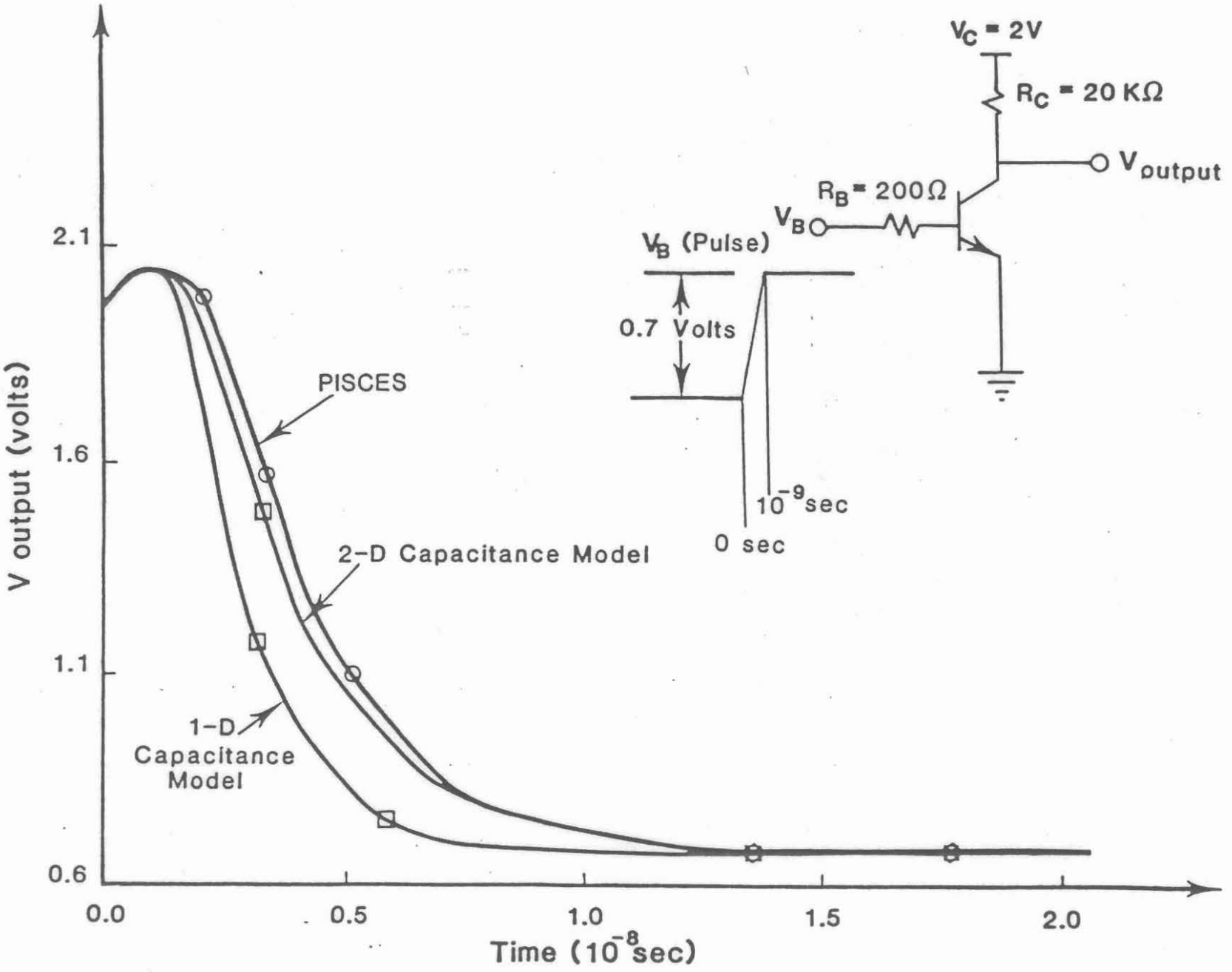
V_C = 2V
R_C = 20 KΩ
V_{output}
R_B = 200Ω
V_B
V_B (Pulse)
0.7 Volts
10^{-9}sec
0 sec
PISCES
2-D Capacitance Model
1-D Capacitance Model
V output (volts)
2.1
1.6
1.1
0.6
0.0
0.5
1.0
1.5
2.0
Time (10^{-8}sec)

Fig. 1