Mixed-Mode SPICE Simulation for Advanced Bipolar TCAD

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Summary

A novel semi-numerical method for mixed-mode (device/circuit) simulation of advanced bipolar (and BICMOS) ICs is presented and demonstrated through a TCAD exercise leading to optimal design of an ECL gate based on a contemporary technology. The method derives from the direct incorporation of a physical and predictive charge-based bipolar transistor model into SPICE2.

This work was supported by the Semiconductor Research Corporation under Contract No. 87-SP-087.

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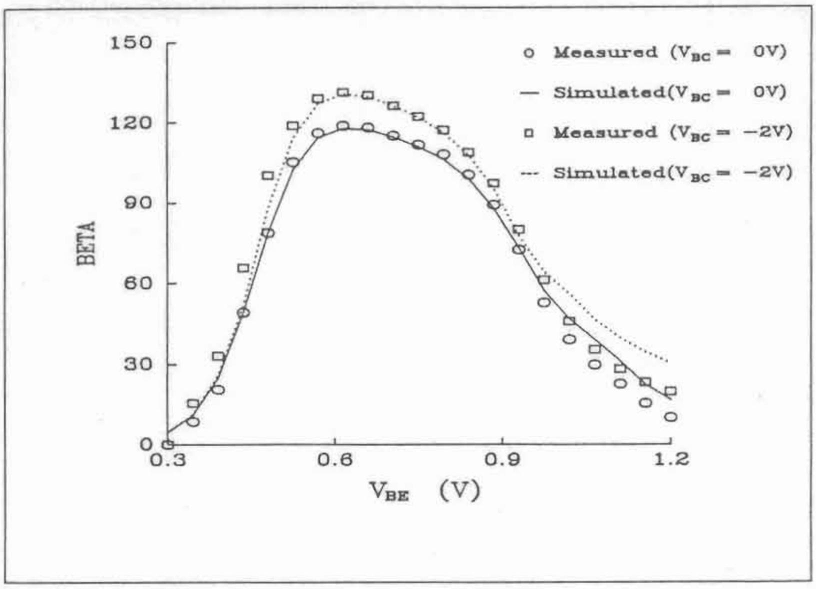
As VLSI technologies advance and submicron feature sizes emerge, technology CAD will require more complex physics-based simulators. Mixed-mode device/circuit simulation, which derives the simultaneous solutions of the coupled device carrier transport equations and the circuit nodal equations, will be necessary for the effective CAD of an IC chip based on yield and reliability as well as performance.

We present a novel, effective method for mixed-mode simulation of advanced bipolar (and BICMOS) ICs that utilizes a physical, semi-numerical bipolar transistor (BJT) model written directly into the circuit simulator SPICE. In contrast to the conventional device simulator, in which the carrier transport (differential) equations are solved numerically, the modified version of SPICE (MMSPICE) contains an analytic but physical characterization of the carrier transport in the BJT which is amenable to numerical solution by the nodal analysis of SPICE. The BJT model is predictive in that the majority of its parameters can be defined directly from process and layout information. Hence MMSPICE, with the BJT model incorporated into the SPICE code, is an effective mixed-mode simulator for advanced bipolar TCAD.

The new large-signal BJT model is charge-based. A set of analytic equations, derived from regional analyses of ambipolar carrier transport in the advanced (double-polysilicon self-aligned) device structure, implicitly describes the current-voltage characteristics and the quasi-static stored charges, the time-derivatives of which properly account for the distributed charge dynamics. Charge partitioning (between the emitter and collector) can give adequate accountings for significant non-quasi-static behavior. Thus the inherent nonreciprocal transcapacitances of the BJT are simulated directly, without the use of equivalent-circuit capacitors. The model is not an equivalent circuit, but is a physical representation of the BJT derived from the underlying transport equations through key analytic approximations and careful coupling of the regional analyses. All significant physical mechanisms, including quasi-saturation (ohmic and non-ohmic), base-width modulation (emitter- and collector-side), and multidimensional current flow (collector spreading, emitter crowding and sidewall injection), are accounted for without resorting to empiricism which would sacrifice the predictive capability of the model.

The model has been verified by measurements of advanced-technology (MOSAIC-III) BJTs fabricated at Motorola (Mesa, AZ) having drawn emitters as small as 1.5 x 4.0 μm^2. The verification involved parameter extraction, which proved to be straightforward because of the physical nature of the model. Many of the 27 model parameters are derived directly from process and layout information; a few are semi-physical (optimized but tightly constrained based on process and layout information) to account for uncertainties in the physics and the device structure, which in fact would exist in direct numerical simulation as well. To exemplify the predictive capability of the model, we show in the figure below measured and MMSPICE-simulated $\beta(V_{BE}, V_{BC})$ characteristics for a device with drawn emitter area of 2.0 x 4.0 μm^2. The agreement is excellent, and the parameter extraction, which required little optimization, was based predominantly on SUPREM simulation of the process and on the device layout.



The semi-numerical BJT model was written directly into the SPICE2 circuit simulator to create MMSPICE. The system of model equations is analytic but implicit, and hence requires numerical solution within each Newton-Raphson iteration of the SPICE nodal analysis to determine the operating-point (V_{BE} and V_{BC}) currents, charges, transconductances, and transcapacitances. Physical properties of the analytic equations and (moving) boundary conditions are exploited in the model numerics to minimize the computational time spent in the model routine. Such optimization of the numerics limits the computational burden of the physical BJT model to approximately an order-of-magnitude above that of the (empirical) Gummel-Poon model in SPICE2, and to about three orders-of-magnitude below that of a corresponding PISCES simulation. The anticipated prodigious advantage in computational efficiency of MMSPICE over conventional numerical mixed-mode simulators like MEDUSA is obvious.

To demonstrate the mixed-mode simulation capability of MMSPICE, we describe a TCAD exercise leading to optimal design of an ECL gate based on the Motorola MOSAIC-III technology. We use MMSPICE to simulate the four-transistor ECL gate, and to predict its delay as determined by the bias conditions, e.g., the on-state BJT current, and by the process parameters, i.e., BJT area, doping densities, junction depths, etc. Consistent with previous designs based on experimental iteration of the fabrication process, we predict that the delay can be minimized (< 80 ps) through proper design of the thin epitaxial collector and by operating at about twice the saturated velocity-limited current density, qv_sN_{epi}.

We stress the relative efficiency of the mixed-mode simulation of advanced bipolar ICs with MMSPICE, which would enable design optimization based on yield and ultimately on reliability, the physics of which could be implemented also semi-numerically. We also stress that the accuracy of this novel semi-numerical mixed-mode simulator is not greatly sacrificed due to the analytic approximations in the BJT model. These approximations are defined from careful consideration of the underlying physics to be commensurate with the uncertainty (viz., noise) in the fabrication process, which in fact implies the yield of the technology.