ADAPTIVE REFINEMENT PRESERVING THE QUALITY OF THE INITIAL GRID

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Summary. *Adaptive grid refinement for semiconductor-device analysis becomes more and more important due to the increasing complexity in the geometrical shape and in the physical models. The technique presented here has the advantage of allowing for anisotropic refinements while preserving smoothness, aspect ratio, matrix bandwith, and minimum number of obtuse triangles of the initial grid.*

Abstract. The adaptive refinement technique has been implemented in two dimensions in an improved version of the grid generator ATMOS [1]. This code is interfaced with the solver HFIELDS [2] which, in turn, is based on the well-known Box Integration Method with a piecewise-linear approximation for the electric potential φ. The basic features of ATMOS are *a)* an automatic refinement of the initial (coarse and rectangular) grid based on the shape of the boundaries and on the dopant distribution and, *b)* the transformation of the rectangular grid into a triangular one. If needed, an interactive refinement is also available. The generation procedure gives rise to a grid having the following properties: *i)* smooth transition in the size of adjacent elements, *ii)* aspect ratio ranging between 0.5 and 2 for the elements having terminating lines (this eliminates the obtuse angles in the interior of the domain), *iii)* minimization or elimination of the remaining obtuse angles (i.e., those along the boundaries), *iv)* regularity in the bandwith of the connectivity matrix (typ. 6 adjacencies with a large majority of right triangles, this reducing the effective adjacencies to typ. 4) and, *v)* special treatment of the boxes surrounding a node where a termination of a grid line occurs. The latter point prevents a spike in the electric potential which typically occurs when the electric field is high in the direction normal to the transition in the grid size (e.g., the direction normal to the channel of a MOSFET near the junction edges).
Some adaptive refinement procedures for semiconductor-device analysis have been presented in the literature [3,4] and are usually based on the behaviour of φ. The procedure presented here is based on φ as well, and has a feature which we believe is very attractive: all the properties *i)* through *v)* above are preserved at any stage of the refinement. This avoids the introduction of "clusters" of slender, and very often obtuse, triangles which increase the matrix bandwith and usually degrade the quality of the grid. The implementation has been carried out by linking ATMOS with HFIELDS' Poisson-solver, by letting the latter code run on the current grid, and by introducing two tests to be repeated on φ at each node and element, respectively, and along both direction x and y. The first test is based on the lower-order term in the deviation from linearity at each node, which in the x direction is $(1/2)\,\varphi_{xx}\,\Delta x^2$. If this test fails, a refinement takes place in the x direction (i.e., the refinement is anisotropic). The key point here is that the refinement does not start from the current grid, which is triangular, but from the corresponding —and previously stored— rectangular one. In this way, properties *i)* through *iv)* above are automatically preserved.
Typically, the position of the terminating nodes mentioned at point *v)* is modified by the refinement. The second test takes place here and is based on one component (along y in the example) of the electric field on the elements surrounding a terminating node. If the test fails, a propagation is forced in the grid line in the x direction. This moves the terminating node to the next element, onto which the test is then repeated. The key point here is that the choice of the electric field component and of the propagation direction is unique, this yielding the result that the terminating nodes are eventually moved outside the high-field region without any degradation in the quality of the grid.
Fig. 1 shows the final grid for a typical 1 μm MOSFET biased at $V_{GS} = 2.0$ V and $V_{DS} = 0$ V. The latter comprises 1,395 grid points and is heavily refined at the source/drain junction curvatures and within the inversion layer. The corresponding electric potential is shown in Fig. 2, and proves the validity of the used refinement criteria. Figs. 3 and 4 represent φ_{xx} and φ_{yy} at an intermediate iteration, which exhibit acute peaks at the Si-SiO_2 interface and at both ends of the channel, respectively. According to our refinement algorithm, the higher the second derivatives of the electric potential, the smaller the element size turns out to be along the corresponding direction. Fig. 5 shows the $I_D - V_{DS}$ curve and the number of nodes corresponding to each bias point and, finally, Fig. 6 shows the effect of a forced propagation of a terminating node in the channel region.

[1] P. Ciampolini, A. Gnudi, R. Guerrieri, M. Rudan, G. Baccarani, ATMOS: *A Mesh Generator for Device Simulation*, NASECODE V Conference, Dublin, 1987

[2] G. Baccarani, R. Guerrieri, P. Ciampolini, M. Rudan, HFIELDS: a *Highly Flexible* 2-D *Semiconductor-Device Analysis Program*, Proc. NASECODE IV, Dublin, 1985
[3] IEEE Trans. Electron Devices, vol. ED-30 (special issue), Sept. 1983
[4] S.P. Edwards, K. De Meyer, Ph. De Wilde, *Adaptive Meshing Applied to a Two-Dimensional Device Simulator*, Proc. NUMOS I, Los Angeles, 1986

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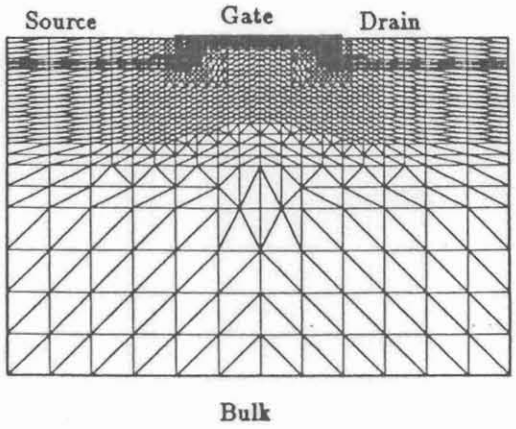

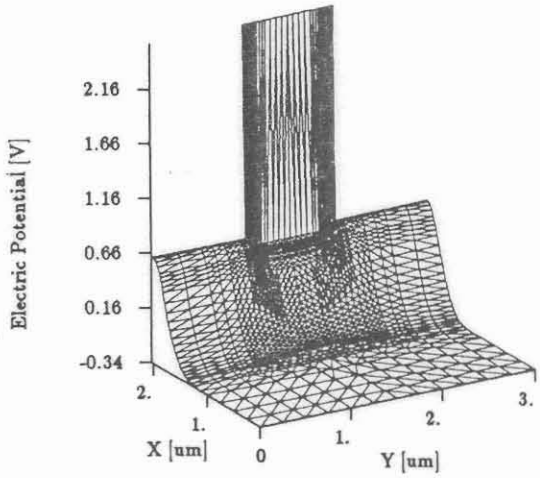

Fig. 2

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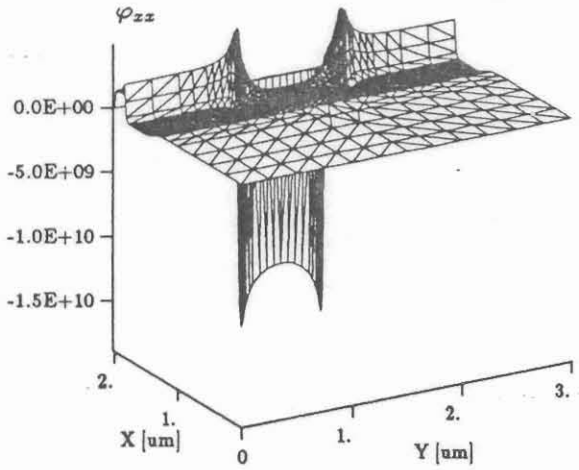

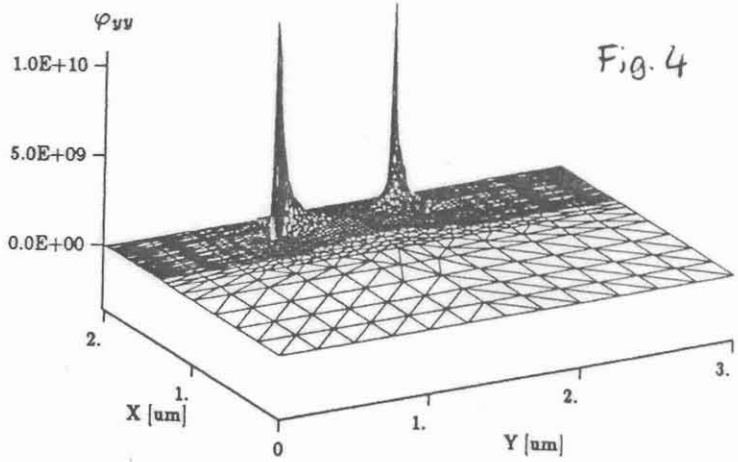

Fig. 4

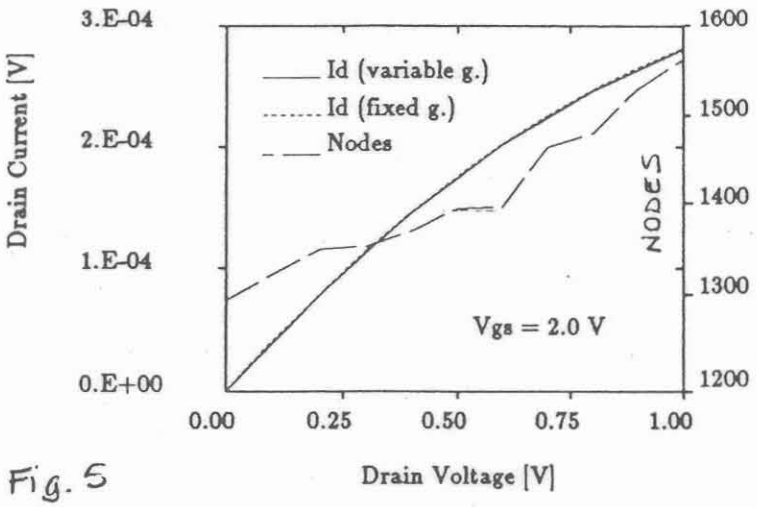

Fig. 5

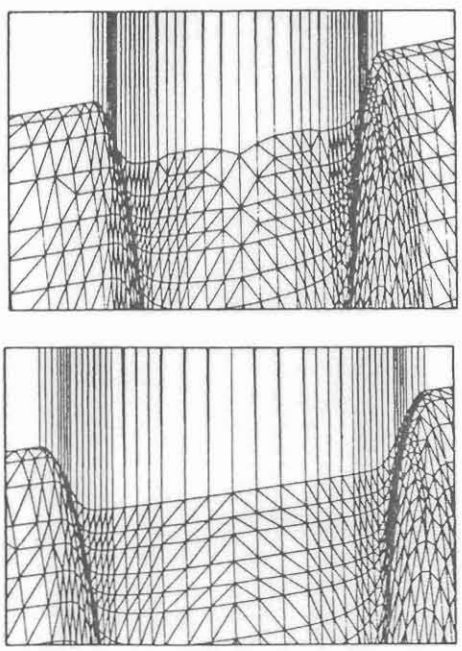

Fig. 6