SIERRA, A 3-D Device Simulator for Reliability Modeling

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The availability of two-dimensional device simulation programs from universities [1,2] has substantially benefitted the semiconductor industry in the simulation of device and reliability effects [3]. However, some important phenomena (*e.g.*, latchup, single-event upset (SEU), and electrostatic discharge (ESD)) are inherently three-dimensional thus requiring even more sophistication from a device simulator. In this paper we describe SIERRA, a full 3D simulator, and its application to latchup in narrow width thyristors typical of CMOS parasitic thyristors, as well as to SEU simulation in closely-spaced trench type capacitors.

SIERRA consists of model generation, solver and post processor functional blocks as shown in Fig. 1. One of the major barriers in 3D simulations is the complexity in constructing three dimensional objects. To surmount this difficulty, we have implemented an integrated system for 3D structure generation. Instead of defining details of the device geometries through a graphics editor, the device structure is extracted directly from the ICE (Integrated Circuits Editor) database. This is accomplished through successive calls to SIMPL-2 [4] to extract material boundary and doping information for multiple parallel cross-sections through the device. The 3D object is then formulated from the collection of cross sections. The advantage of this approach is twofold. First, it removes the burden of model construction from the engineer. Secondly, the extraction of material boundaries directly from process simulations results in a more accurate structure. This is especially important in determining coupling capacitances where an accurate geometry is required. An example of two metal lines crossing is shown in Fig. 2.

The equation solver was built using the basic framework of PISCES-2B [1]. The Poisson and electron and hole current-continuity equations are discretized using triangular prismatic elements. The triangular surfaces of the elements are used to discretize the planes containing the major axes of the device operation while rectangular elements are used in the remaining direction. This approach preserves the efficiency and flexibility of triangular mesh to effectively model the material boundary or doping changes and avoids the complication of tetrahedral elements. Two methods are commonly used to solve the system of linearized equations. The Gummel method iteratively solves the Poisson and continuity equations. The approach is very effective in the low current regions where the coupling beween Poisson and continuity equation is weak. The ICCG method has shown a greater efficiency than the direct elimination method in solving the 3D Poisson equation. The increased sparsity in 3D simulation has made ICCG method more appealing. However, the Gummel/ICCG method loses its effectiveness as the coupling between Poisson and

continuity equations increases. Under high injection condition, the full Newton method is more robust and efficient. The performance comparisons of various numerical methods for the 3D simulator will be presented.

One objective for developing the 3D device simulator pertains to reliability simulation and modeling. Specifically, CMOS latchup, SEU, and ESD require 3D simulators for full characterization. SIERRA was first applied to study the narrow width and proximity effects on latchup immunity. As an example, the device was first reverse biased to 5V using the Gummel/ICCG method. The potential contour is shown in Fig. 3. The device was triggered by flooding electron-hole pairs across well junctions at zero time. Finally, after 1 nsec, the transient reached the steady state situation in which the device was in the latched state (Fig. 4). The holding point was reached by stepping the voltage down until the turning point in the I-V curve was found. The potential contour at the holding point (Fig. 4) illustrates the 3D effects.

SIERRA was also applied to simulate the alpha-particle-induced charge transfer between two closely spaced trench type capacitors [5]. Fig. 5 shows the potential contour indicating the current path formed along the particle track. The particle track was eventually pinched-off near the junction of the higher biased node. The physical mechanisms are similar to the 2D simulations; however, the time scale is shortened due to the reduced spreading resistance observed in the 3D structure. The comparison of currents as functions of time for both the 2D and 3D simulations is shown in Fig. 6.

References

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4. Keunmyung Lee, *SIMPL-2 (Simulated Profiles from the Layout – Version 2)*, PhD. Thesis, University of California-Berkeley, 1985.

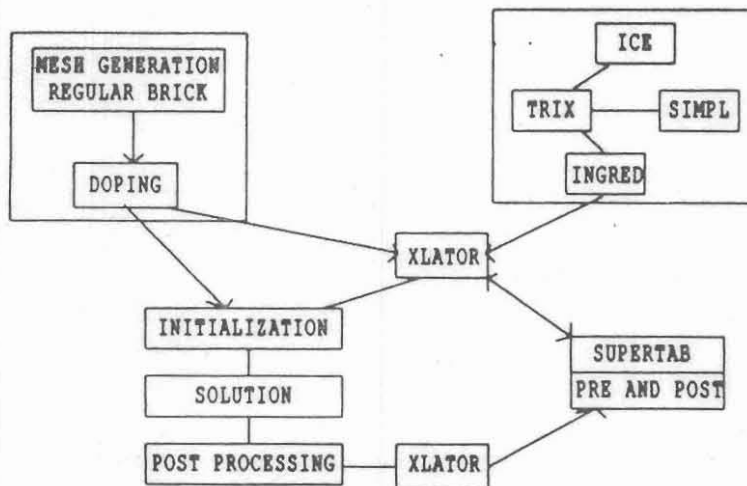

Fig. 1: Block diagram of SIERRA.

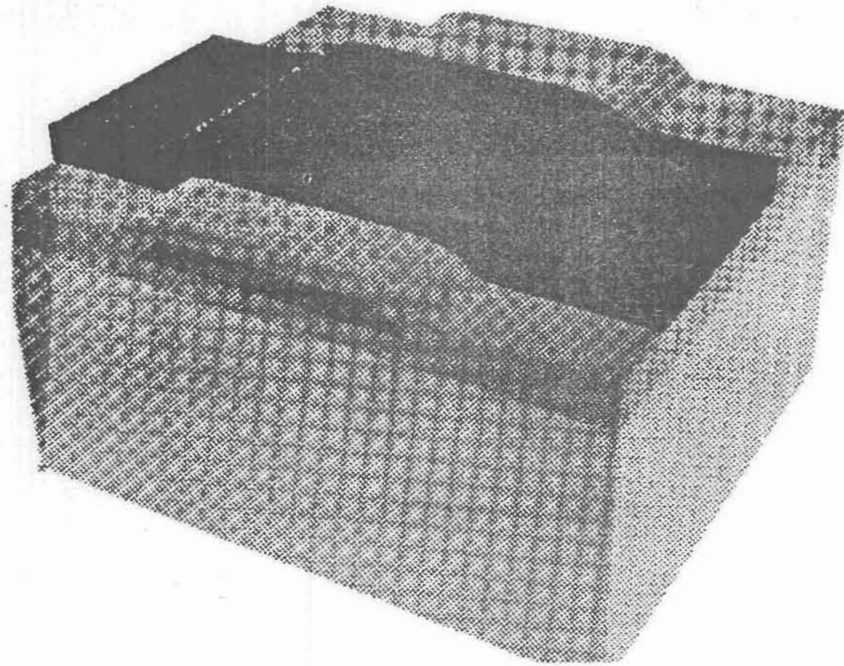

Fig. 2: 3D interconnect model

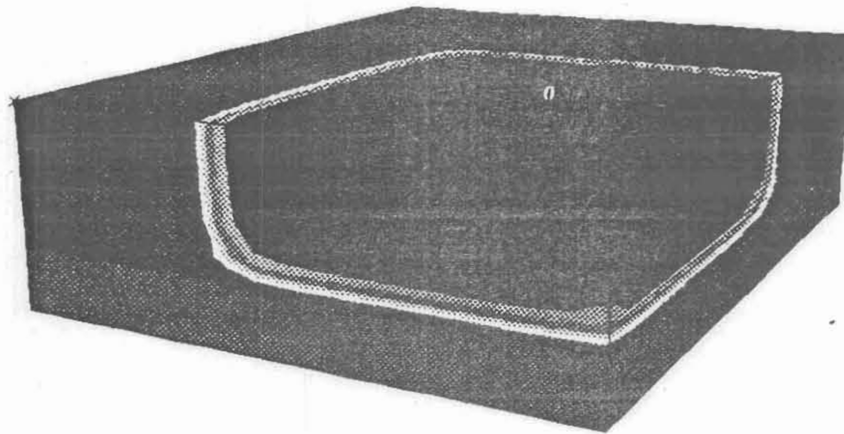

Fig. 3: Parasitic thyristor potential profile at $V_{DD} = 5V$.

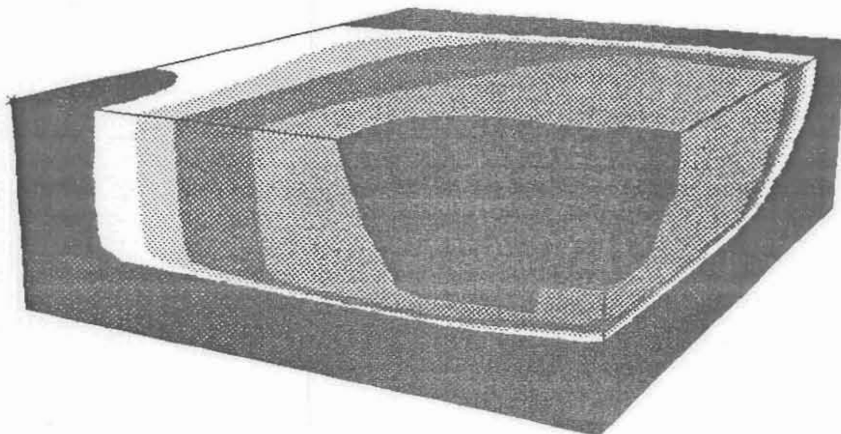

Fig. 4: Parasitic thyristor in latched state.

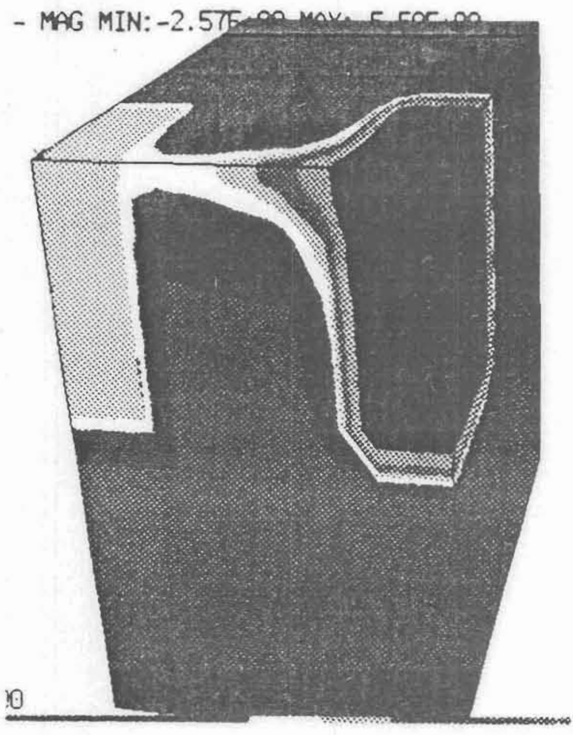

Fig. 5: Closely-spaced trench capacitor cells showing charge transfer induced by alpha particle.

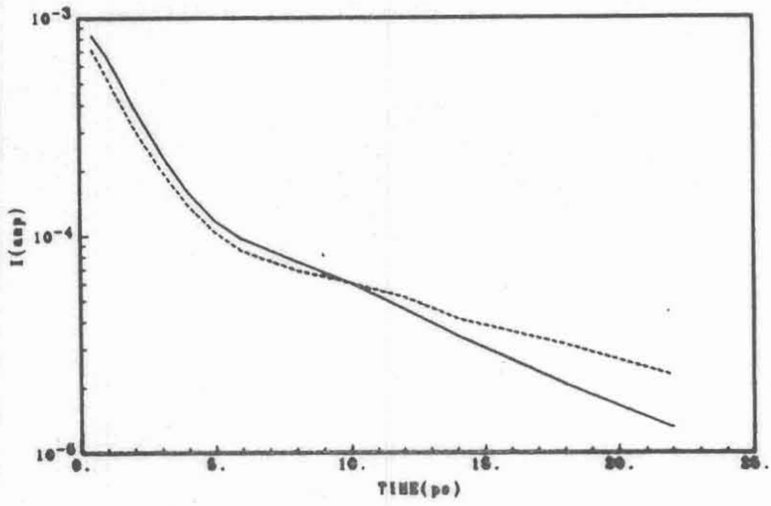

Fig. 6: Transient current from 2D (dashed) and 3D (solid) simulations.