Hot Carrier Analysis in Sub-0.1 μm GaAs MESFET

D.Y. Cheng, C.G. Hwang, D.R. Allee, R.F.W. Pease, and R.W. Dutton
AEL 231, Integrated Circuit Laboratory, Stanford University

Abstract

PISCES-MC, a multi-window multi-method 2D device simulator has been developed to analyze hot electron effects[1] . It has been applied to a GaAs MESFET with 920 Å recessed gate, and the simulation results are in good agreement with measured data. Proper window boundary selection and contact placement are critical to obtaining high accuracy results. To provide high speed simulation, the program has been adapted to both shared memory and the Hypercube multiprocessors.

A GaAs MESFET with 920 Å recessed gate has recently been fabricated[2] . The drift-diffusion equations cannot model the devices of this size. To simulate this device the PISCES algorithm is used to provide an initial guess and boundary conditions for a Monte Carlo simulation of the critical portion of the device, as shown in figure 1. Figure 2 and figure 3 compare the experimently measured I-V characteristics and the simulated results. The difference is below 8.4%. Experimently measured extrinsic DC transconductance at Vg = 0V has a value between 220 and 250 ms/mm[2] ; simulation gives 218 ms/mm. The predicted unity current gain frequency of the device (based on the relation $f_T = g_m/2\pi C_g$), is 76 GHz. Simulation shows that the forward bias gate current of the device is negligible when Vd <= 4V, Vg = 0V, but rises to 0.11 mA/μm at Vg = 1V. Velocity overshoot exists in the channel under the gate over a distance of 1000 Å. The simulated average electron velocity in the channel is 1.29×10^7 cm/sec at Vg = 0.2V and Vd = 3V, 1.11×10^7 cm/sec at Vg = -0.2V, Vd = 3V. These average electron velocities are not substantially higher than the value found in large gate length devices[3] , and agree with the experimentally determined value of 1.2×10^7 cm/sec for this device[2] .

The window boundary and window contact placement are critical to obtaining more accurate results. To account for the retarding field near the source contact properly, the injecting boundary (window source boundary) should be placed at a location where both electric field and its spatial derivative are small. When this boundary is placed at the peak electric field, the drain current is 37.5% lower than the measured value, and the average carrier velocity is lower as well. This difference is partially caused by the fact that the particles injected from this boundary do not experience the full retarding field. This shows that under low gate bias conditions, placing the injecting boundary slightly away from the peak retarding field toward the source contact gives accurate results. When the retarding field is very high however, the probability of a particle to surmount the barrier is very low and the number of particles needed to obtain a reasonable simulation result is prohibitive. In this situation placing the injecting boundary at the peak retarding field provides a way to obtain insight into device performance[4] .

At the collecting boundary (window drain boundary) the number of particles transferred into the upper valleys must be negligible[1] . The drain current and therefore the g_m and f_T are sensitive to the drain contact size, although the average carrier velocity and energy are not. For devices with complicated geometry the Monte Carlo window may not connect to the physical contacts on the device as shown in figure 1. In this situation the window contact lengths and directions should be adjusted to account for current continuity.

For this example at one bias point, the program takes approximately 2 hours on a Convex-C1 and 1.3 hours on a single processor Alliant. By using a multiprocessor version of the algorithm on an 8-processor Alliant, this time is reduced to 11 minutes! The program has shown nearly perfect speedup on a 20-processor shared memory machine (Sequent) and on an Intel 16-processor Hypercube. Table 1, 2, and 3 summarize these results.

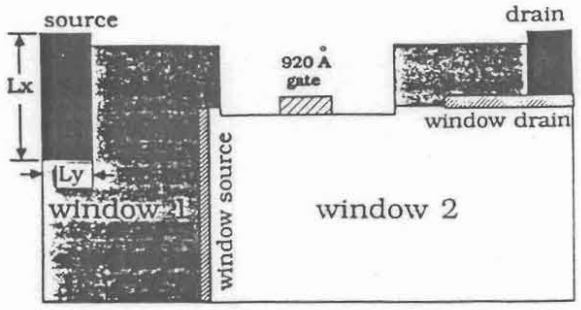

Fig. 1. Simulation windows and contact placement.
Window 1: PISCES-IIB, Window 2 : Monte Carlo

Multiprocessor Speed-up on Alliant FX/8			
Number of processors	CPU Time (min)	Speed Up	Efficiency
1	79.1	1.0	100%
2	40.2	1.97	99%
4	20.8	3.81	95%
6	14.7	5.37	90%
7	12.9	6.15	88%
8	11.4	6.96	87%

Table 1: A simulation with 12K particles and 100 time steps with scalar optimization

Multiprocessor Speed-up on Sequent Balance 8000			
Number of processors	CPU Time	Speed Up	Efficiency
1	81 hr 5 min	1	100%
4	20 hr 41 min	3.95	98.8%
6	13 hr 44 min	5.91	98.4%
8	10 hr 22 min	7.82	97.8%
12	6 hr 58 min	11.64	97.0%
16	5 hr 21 min	15.15	94.7%
20	4 hr 23 min	18.50	92.5%

Table 2: A simulation with 12K particles and 100 time steps without optimization

Multiprocessor Speed-up on iPSC			
Number of processors	CPU Time	Speed Up	Efficiency
1	16 hr 28 min	1.0	100%
2	8 hr 23 min	1.97	98.5%
4	4 hr 20 min	3.83	95.8%
8	2 hr 19 min	7.26	90.7%
16	1 hr 19 min	13.0	81.4%

Table 3: A simulation with 12K particles and 100 time steps

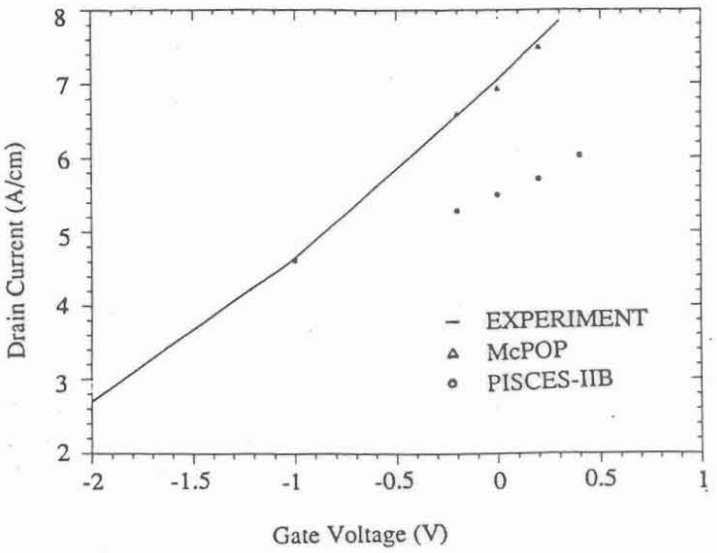

Fig. 2. Drain current versus drain voltage at Vg = 0V

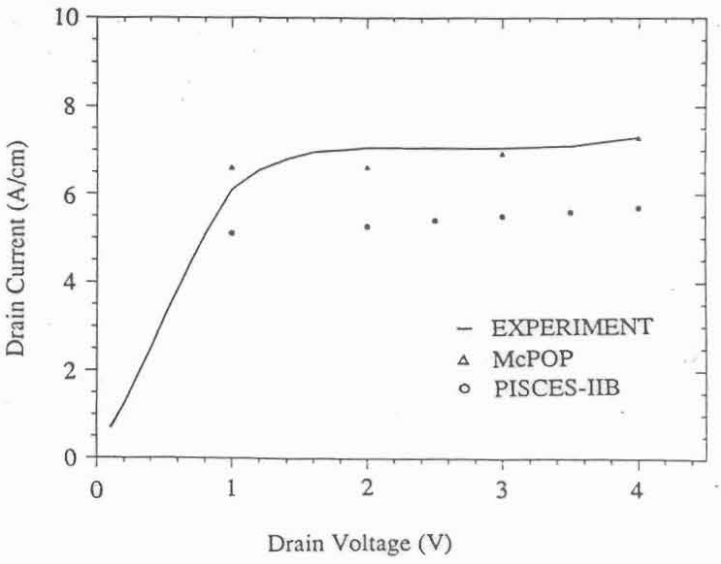

Fig. 3. Drain Current versus gate current at Vd = 3V

1. C.G. Hwang, D.Y. Cheng, H.R. Yeager, and R.W. Dutton, "Multi-Window Device Analysis of Hot Carrier Transport," *IEDM*, pp. 563-566 (1986).

2. D.R. Allee, P.R. de la Houtssaye, D.G. Schlom, J.S. Harris, and R.F.W. Pease, "Sub-0.1 μm Gate Length GaAs MESFETS Fabricated by a Combination of Molecular Beam Epitaxy and Electron Beam Lithography," *Vac. Sci. & Technology B*, (to appear).

3. L.F. Eastman, "The Physical Electronics of High Speed Transistors," *Proc. IEEE/Cornell Conf. Advanced Concepts in Semicond. Dev. and Circuits*, pp. 1-10 (July 29-31, 1985).

4. P.T. Nguyen, D.H. Navon, and T.W. Tang, "Boundary Conditions in Regional Monte Carlo Device Analysis," *IEEE Trans. Electron Devices* **ED-32 No. 4** pp. 783-787 (April, 1985).