Gallium Arsenide Transistor Engineering modelS: GATES

R. Anholt* and T.W. Sigmon
Solid State Electronics Laboratory, Stanford University, Stanford Ca. 94305
*Present address: 1030 Sixth St. SE, Minneapolis, Minn. 55414

A combined process and device modeling package for GaAs MESFET IC technology is described. The presented paper will discuss models used to obtain device electrical characteristics of ion-implanted MESFET's, comparisons between the model and measurements, and a few applications to the consideration of device performance and uniformity.

GATES is designed to meet the everyday needs of the process, test, and manufacturing engineers, who require the answers to questions about how process parameters and tolerances affect device performance and uniformity, but who have limited access to large-computer modeling tools. GATES is designed to be an easy-to-use, interactive tool, running efficiently on AT-type personal computers (or VAX's under VMS).. To achieve this performance, extensive use is made of analytical models.

GATES features calculations of

- Accurate Ion-Implant Profiles, obtained by fitting extensive SIMS measurements
- Recess etching and epitaxial layers
- Dopant diffusion during annealing
- LEC and HB wafer-impurity effects
- Piezoelectric effects
- Short-channel effects, due to n^+ implant encroachment in self-aligned processes
- Poisson calculations of carrier profiles and threshold voltages
- Quasi-two-dimensional calculations of source-drain currents, using the two-piece mobility approximation
- Small-signal parameters: Q_g, C_{gs}, C_{dg}, g_m, g_d, f_T, f_{max}
- Contact, source, and drain resistances
- Simulations of C-V carrier and FATFET mobility profile measurements

The code is primarily interactive, but a batch mode of operation is also available for device optimization. Database generation, reporting, and plotting are also available.

A few applications we have considered are

- Sensitivity of threshold voltages to fluctuations in encapsulant thickness (when implants are made through Si_3N_4 or SiO_2 caps).
- Sensitivity of threshold voltages to gate-recess etch depth fluctuations
- Optimizing the performance of enhancement-mode MESFETs by
  - Using shallower implant profiles
  - Deep-recess etching
  - Buried p layers
- Use of buried p layers to reduce the sensitivity of devices to fluctuating background acceptor concentrations
- Effects of Si knock-on recoils on device threshold voltages when implants are made through caps
- Sensitivity of threshold voltages and transconductances to implant tilt and rotation angles
- Effects of diffusion during annealing on device threshold voltages
- Study of the effects of background EL2, Cr, and C concentrations on threshold voltages, electron profiles, and transconductances

This work was supported by Wright Patterson Air Force Materials Laboratory contract F33615-85-C-5048 (W. Mitchel).

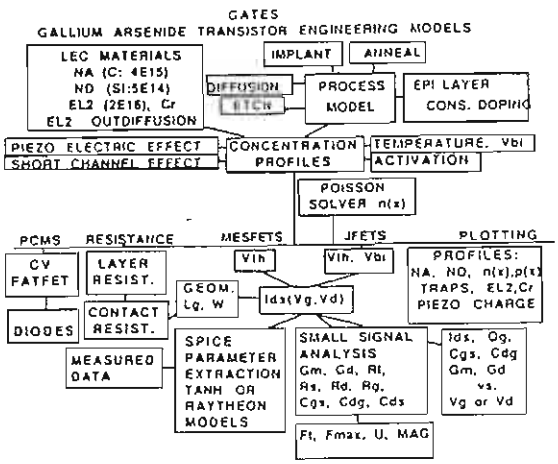


Fig.1. Overview of GATES.

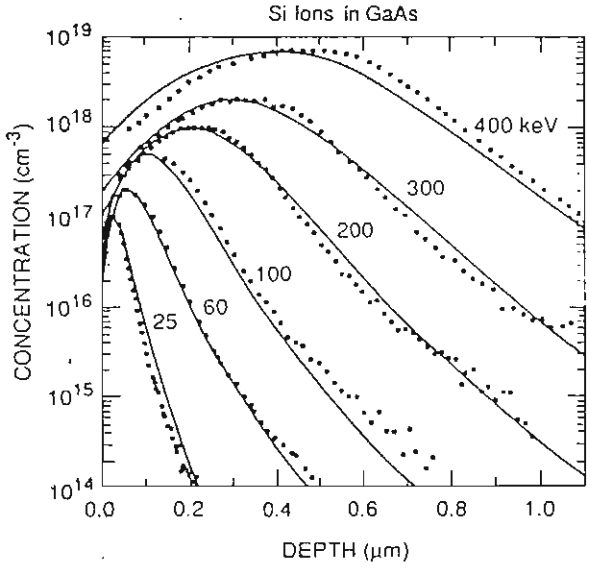


Fig.2 Comparison of SIMS measurements of Si ions implanted into GaAs with Pearson-IV fits, used by GATES.

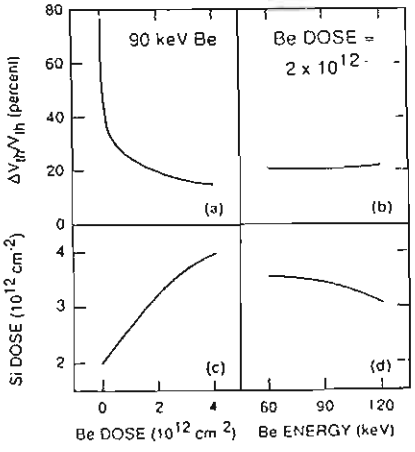
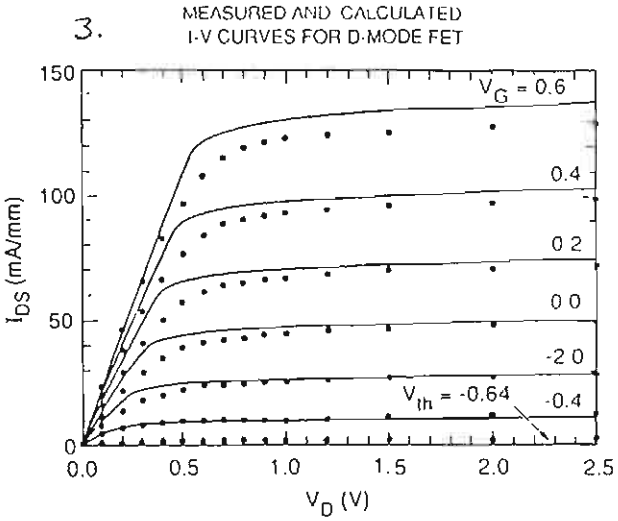


Fig.6 LEC-grown GaAs has uncontrolled C acceptor impurities ranging from 1 to $6\times10^{15}cm^{-3}$, which leads to shifts in the threshold voltage from wafer to wafer. By using a buried p layer, formed by implanting 0.5- to 4×10^{12} 60- to 120-keV Be ions/cm^2, one can reduce the C-induced shift in threshold voltage.



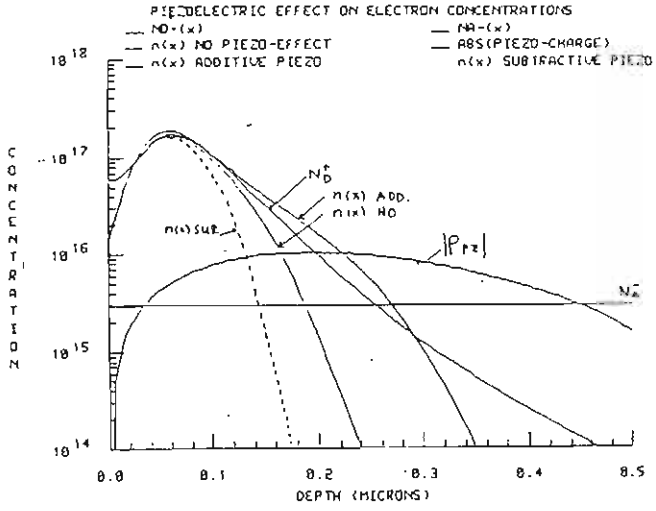


Fig 4 Stress from dielectric films between the source (or drain) and gate electrodes induces piezoelectric charges in GaAs. Depending on the sign of the stress and the orientation of the gate, these charges either add or subtract from the donor concentration, which in turn narrows or broadens the carrier profile at short gate lengths (0.5μm in this example).

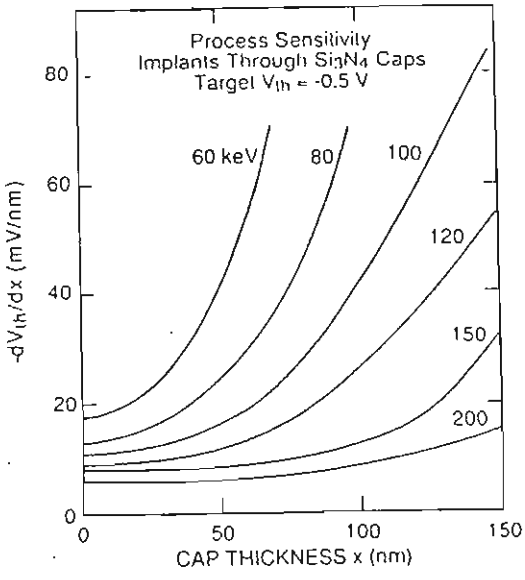


Fig 5. For implantation through dielectric caps, fluctuations in the cap thickness leads to changes in device threshold voltages. Shown is the change in threshold voltage with cap thickness for 60- to 200-keV Si ion implants, where the ion dose was adjusted to achieve a constant -0.5V threshold voltage.