Analytical Models of Ferroelectric Field Effect Transistor with Two-Dimensional Channel Material

Jeonghyeon Kim, and Jiwon Chang
Department of Electrical Engineering, Ulsan National Institute of Science and Technology, Ulsan 44919, Republic of Korea
jiwon.chang@unist.ac.kr

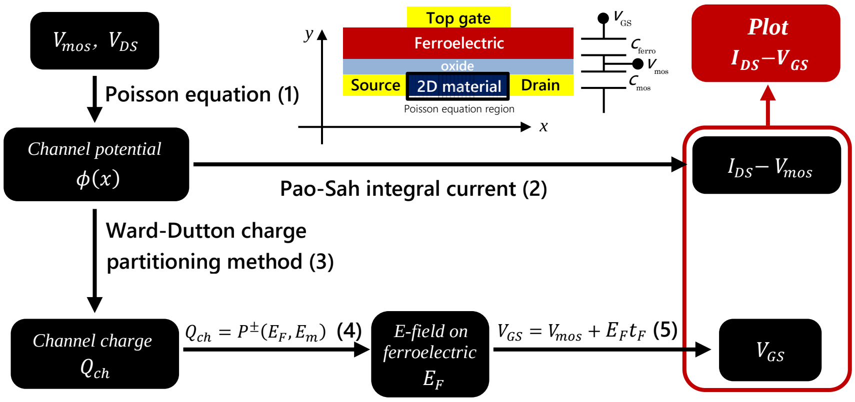
Ferroelectric non-volatile memory has been extensively investigated due to the promising properties such as low-voltage and low-power consumption. In order to analytically understand the electrical characteristics of Si-based ferroelectric field-effect transistor (FeFET), mathematical models have been suggested by Miller et al. [1]. Meanwhile, two-dimensional (2D) transition metal dichalcogenides (TMDCs) have emerged as a promising channel material in ultra-scaled FET due to the atomically thin nature. Accordingly, there have been several experimental demonstrations of FeFET with 2D channel material (2D FeFET), but little development of analytical models to describe the behavior of 2D FeFET.

Here, we present analytical models of 2D FeFET which are developed by modifying Miller's FeFET model using the Poisson equation [2,3] rather than using the Brews charge sheet model [1]. In order to obtain the channel charge in 2D TMDCs, Ward-Dutton charge partitioning method adopted by Jiang et al [2] is used. To explain FeFET behavior more precisely, the mathematical model to describe the non-saturated hysteresis loop of ferroelectrics is adopted [4]. We consider Metal-Ferroelectric-Insulator-Semiconductor (MFIS) structure for 2D FeFET which could be constructed using $CuInP_2S_6$ (CIPS), h-BN and WSe_2 as 2D ferroelectric, 2D insulator and 2D channel materials, respectively. Models for 2D FET without ferroelectrics are also presented to be compared with 2D FeFET and clarify how 2D FeFET works.

We study the dependency of memory window in 2D FeFET on the ferroelectric properties (remnant polarization P_r and coercive field E_c), thickness and dielectric constant of ferroelectric and insulator. Consequently, our work aims to present the optimized 2D FeFET structure that can maximize the memory window.

Acknowledgement: This research was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science, ICT & Future Planning (2020R1F1A1069417).

[1] S. L. Miller and P. J. McWhorter, J. Appl. Phys. **72**, 5999 (1993)
[2] C. Jiang et al., IEEE J. Electron Devices Soc. **6**, 189 (2018)
[3] W. Cao et al., IEEE Trans. Electron Devices, **61**, 4282 (2014)
[4] Hang-Ting Lue et al., IEEE Trans. Electron Devices, **49**, 1790 (2002)



Poisson's equation:

$$\frac{d^2\phi}{d^2x} - \frac{d^2\phi}{d^2y} = \frac{q(n_{2D} - N_d)}{\varepsilon_{2D} t_{2D}}$$

$\phi(x)$: *Electrostatic potential of the channel along x direction*

V_{ch}: *Applied voltage on the channel along x direction*

$$\frac{d^2\phi}{d^2x} - \frac{\phi}{\lambda^2} + \xi = \frac{q(n_{2D} - N_d)}{\varepsilon_{2D} t_{2D}}$$

$$\phi(x) = V_{ch} + \frac{k_B T}{q} ln\left\{\frac{\varepsilon_{2D} t_{2D}}{q n_{2D}}\left[\xi - \frac{\phi(x)}{\lambda^2}\right] + \frac{N_d}{n_{2D}}\right\} \quad where\ \xi \equiv \frac{V_{mos} - V_{FB}}{\lambda^2}, \quad \lambda \equiv \sqrt{\frac{\varepsilon_{2D} t_{ox} t_{2D}}{\varepsilon_{ox}}} \qquad (1)$$

Pao-Sah integral current:

$$I_{DS} = \mu_n \frac{qW}{L}\int_0^{V_{DS}} n_{2D}\, dV_{ch} = \mu_n \frac{qW}{L}\int_0^{V_{DS}}\left[N_d + \frac{\varepsilon_{2D} t_{2D}}{q}\right] d\phi \frac{dV_{ch}}{d\phi} \qquad (2)$$

Ward-Dutton charge partitioning method:

$$Q_{ch} = qW\int_0^L (n_{2D} - N_d)dx = qW\int_0^L (n_{2D} - N_d)d\phi(x)\frac{dx}{d\phi(x)} \qquad (3)$$

P-E hysteresis loop analytical model for a MFM structure:

$$P^{\pm}(E, E_m) = P_S\, tanh\left(\frac{E \mp E_c}{2\delta}\right) + \varepsilon_F \varepsilon_0 E \pm \frac{P_S}{2}\left(tanh\left(\frac{E_m + E_c}{2\delta}\right) - tanh\left(\frac{E_m - E_c}{2\delta}\right)\right) \qquad (4)$$

Modified Gate Bias:

$$V_{GS} = V_{mos} + V_F = V_{mos} + E_F t_F \ , \ where\ Q_{ch} = P^{\pm}(E_F, E_m) \qquad (5)$$

Fig1. Schematic device structure and a modeling flow of 2D FeFET with modeling equations.

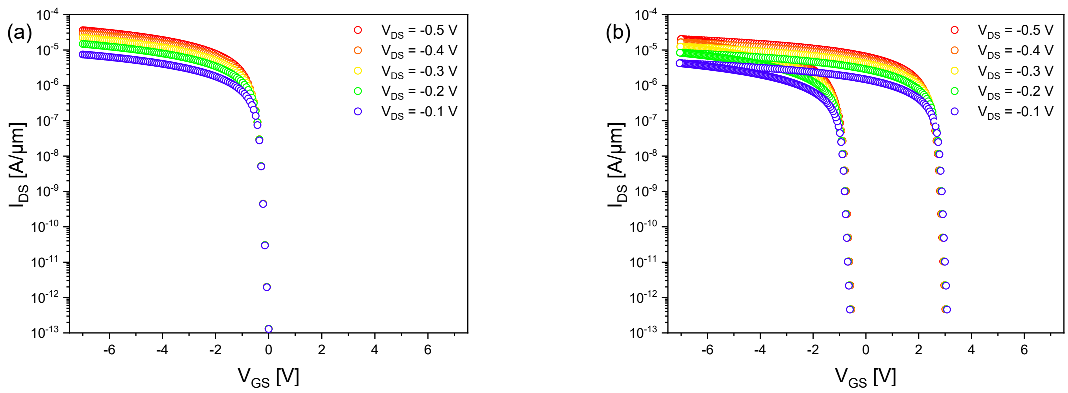


Fig2. Simulated transfer characteristics for 2D FET with gate stack of WSe_2/h-BN (a), FeFET with gate stack of WSe_2/h-BN/CIPS (b).

ISBN 978-89-89453-30-7