## Analogue computing with resistive memory devices

Daniele Ielmini Politecnico di Milano, Italy

**Abstract**: In the era of artificial intelligence, unconventional computing attracts an increasing interest to accelerate sensing and computation by taking advantage of novel devices and novel architectures. Among these unconventional concepts, in-memory computing (IMC) shows the ability to accelerate computation by minimizing data movement and improving the parallelism. A key enabling technology for IMC is the matrix vector multiplication (MVM) in a crosspoint memory array of memory devices, such as resistive switching memory (RRAM) or phase change memory (PCM). MVM is currently being explored for novel accelerators of deep neural network (DNN). Recently, it has been shown that MVM can be extended to a wider class of linear algebra operations, including solution of linear set of equations (Ax = b), matrix inversion, eigenvector calculation and various types of regression, all executed in one step in the analogue domain. Given the ubiquitous nature of linear algebra in modern data processing, the new wave of analogue IMC operations is extremely promising for accelerating computation in many applications. This work presents the status of analogue IMC with resistive memory devices, discussing the underlying concept and the technology, addressing the time response, accuracy, stability and complexity. The underlying opportunities, potential applications and challenges from the viewpoints of device, circuit and architectural will also be discussed.

## **Keywords:**

In-memory computing, resistive switching device, analogue computing

## Bio:

Daniele Ielmini is a Professor at the Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Italy. He received the Ph.D. from Politecnico di Milano in 2000. He held visiting positions at Intel Corporation and Stanford University in 2006. His research interests include the modeling and characterization of non-volatile memories, such as phase change memory (PCM), resistive switching memory (RRAM), and spin-transfer torque magnetic memory (STT-MRAM). He authored/coauthored more than 300 papers in international journals and conferences. He is Associate Editor of IEEE Trans. Nanotechnology and Semiconductor Science and Technology (IOP). He received the Intel Outstanding Researcher Award in 2013, the ERC Consolidator Grant in 2014, and the IEEE-EDS Paul Rappaport Award in 2015. He is a Fellow of the IEEE.

