Temperature Dependent Electrical Characteristics and Single Charge Trap Induced by Random Telegraph Noise of Bulk FinFETs

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We for the first time study temperature dependent random telegraph noise (RTN) of bulk fin-type field effect transistors (FinFETs) induced by acceptor-type single-charge trap for sub-7-nm technologies. The significant reductions of off-state current of the explored bulk FinFETs under the reduced temperature and its enhanced device performance in terms of I_{on}/I_{off} ratio. For bulk FinFETs, the trap position at middle of the channel with different temperature, the RTN magnitude (($\Delta I_D/I_D$) × 100%) is estimated. The impact of RTN is significant under the cryogenic (low) temperature.

Bulk FinFET has been the dominant technology on the VLSI technology for emerging electronic applications. It has the wonderful electrostatic control, effective immunity of short channel effects and CMOS comparable manufacturability [1]. The prediction of ITRS 2.0 roadmap [2], the FinFETs will continuous scaling trend of CMOS transistors to sub-5-nm technology nodes and beyond. As lowering the ambient temperature, the device performance improves in terms of I_{on}/I_{off} ratio and steeper subthreshold swing [3]. In this work, we computationally study the device transfer characteristic (I_D-V_G) with different temperatures. RTN influenced by acceptor-type single charge trap (SCT) presenting at middle of the channel between the silicon channel and gate dielectric is calculated with respect to different temperatures for bulk FinFETs by using the experimentally validated 3-D device simulation [4]. The magnitude of RTN induced by 3-D SCT having both length and width of 2-nm and 0.5-nm height locating middle of the channel [5-6]. At the high temperature due to low carrier mobility, the reduction of RTN is caused. By extracting SCE parameters, we discuss characteristic variability induced by SCT. We observe that the magnitude of RTN is high at low temperature.

Figure 1 illustrates the simulated 3-D structure for the nominal bulk FinFET with specified regions. The simulated device physical parameters with regions are listed in Table I. The device having 16-nm gate length with gate stack of Ti/HfO_2/SiO_2 and silicon. This simulation is examined by solving 3-D quantum-mechanically corrected density gradient model along with drift diffusion model, which is valid, by nonequilibrium green function [4]. We express the simulation results of the temperature varying from high to low, the transfer characteristics can be boosted, especially in terms of off-state current reduction as shown in Fig. 2. It is evident by observing the conduction band profile along the channel from source (S) to drain (D), as depicted in Fig. 3. The low temperature has a high off-state conduction barrier which leads to lower leakage at off-state and boost the device performance. The high-temperature device possesses the lower barrier, compared with the low-temperature one. To explore the most severe impact of the SCT on RTN, we further consider the density of interface trap of 10^{12} cm^{-2} eV^{-1}. Figure 4 illustrates the calculated magnitude of the RTN in the presence of SCT (by calculating the deviation $\Delta I_D/I_D$ x 100%.) due to trapping/de-trapping, where the SCT is positioned in the middle of the channel with different temperatures. The magnitude of RTN decreases with increasing V_G due to the low charge carriers. Finally, the RTN magnitude is large at low temperature because the increased carrier mobility causes to enhance the charge capture and emission rate of SCT [5]. From the RTN magnitudes comparison with respect to different temperature, the decreased temperature causes to an increased RTN magnitude. It is noticed from the off-state conduction band profile in the channel under the presence of SCT, the barrier height is enhanced with the reduced temperature; thus, it causes to high SCT fluctuation, as shown in Fig. 5.

In summary, we have investigated the SCT induced RTN for devices under different temperatures. Low-temperature operation can reduce the leakage and boost the device characteristics, but the magnitude of RTN becomes significant (about 40%) for devices operated at low temperature.

Acknowledgement

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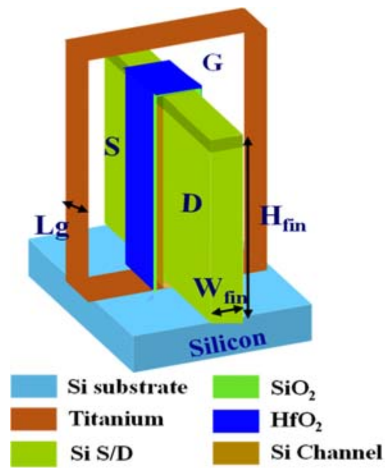

Fig. 1: A 3-D schematic structure of the explored 16-nm-gate (corresponding to sub-5-nm technological node) bulk FinFET with titanium gate metal and HfO_2/SiO_2 and silicon as gate stack and the regions are specified in appropriate color.

Tab. 1: List of the N-type nominal bulk FinFET device parameters, the regions and their specified values used in this simulation. Notice that the values presented here were calibrated with experimentally measured data for the best of simulation accuracy.

Device parameter	Value
Channel length (nm)	16
Channel doping (cm^{-3})	5×10^{17}
S/D extension (nm)	5
S/D length	12
Fin height (nm)	32
Fin width (nm)	8
Aspect ratio (Fin height / Fin width)	4
Work function (eV)	4.52
EOT (nm) ($T_{sio2}+T_{hfo2} \times e_{sio2}/e_{hfo2}$)	0.963
S/D doping (cm^{-3})	1×10^{20}
S/D extension doping (cm^{-3})	4.8×10^{18}

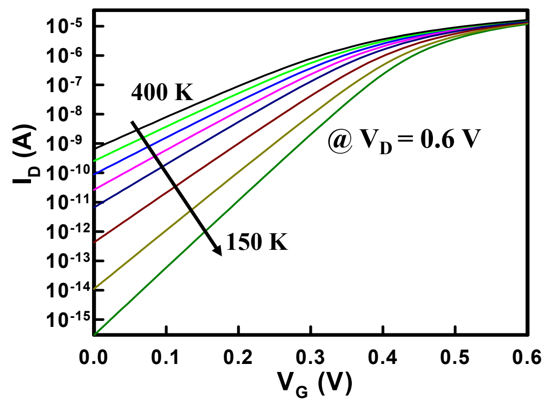

Fig. 2: The transfer characteristics (I_D-V_G) of the simulated bulk FinFET devices with respect to different temperature from high (400 K) to Low (150 K) at V_D = 0.6 V.

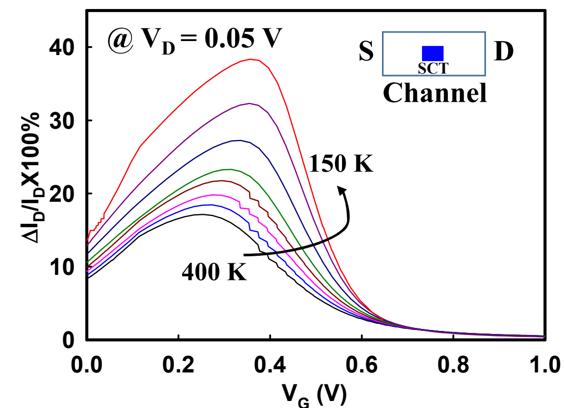

Fig. 4 The calculated magnitude of the random telegraph noise in the presence of the acceptor-type single charge trap at the middle of channel with varied temperature for the device at V_D=0.05 V.

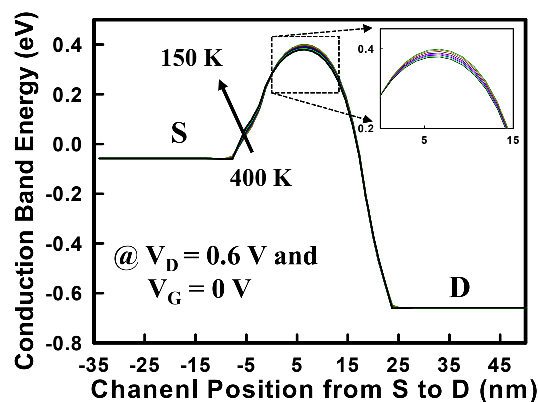

Fig. 3: Plot of the conduction band profile along the channel direction from source to drain with varied temperature from 400 K to 150 K under the off-state condition (V_D = 0.6 V and V_G = 0 V). The inset shows the zoom-in plot at the dotted area.

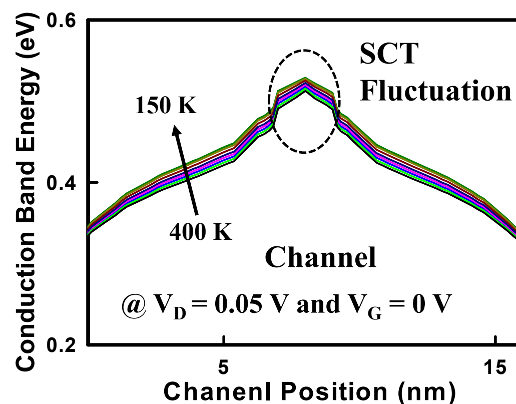

Fig. 5: The off-state (V_D = 0.05 V and V_G = 0 V) conduction band profile of the channel under the presence of SCT locating at the middle of channel with varied temperature, the inset circle represent the SCT induced fluctuation in the conduction band energy profiles.