Computational Research of CMOS Channel Material Benchmarking for Future Technology Nodes: Missions, Learnings, and Remaining Challenges

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In this abstract, we review our journey of doing CMOS channel material benchmarking for future technology nodes. Through the comprehensive computational research for past several years [1-7], we have successfully projected the performance of various novel material CMOS based on rigorous physics models, and we have also obtained new physical insights and learnings on the key design considerations for extremely scaled n- and pMOS transistors. There are, however, still research gaps and challenges remaining to complete the whole picture and provide an ultimate theoretical guidance on the material choice for future CMOS, as will be discussed at the end of this abstract.

For the model device, we considered double-gate (DG) or gate-all-around (GAA) nanowire (NW) MOSFETs with the gate length (L_G) of 13 nm for various n- and pMOS materials (**Fig. 1**). We first showed that it is essential to optimize the device design depending on each material. As shown in **Fig. 2**, it is critical to optimize the source/drain (S/D) design such as the tip doping density (N_{tip}) to balance the source exhaustion [8] vs. tunneling leakage for materials with small effective mass (m^*) and bandgap, such as III-V's and Ge [1, 9]. For materials with multiple valleys (Γ, L, and X), it is also important to optimize the crystal orientation [10, 11]. In **Fig. 3**, we show that quantum confinements in Ge NW nMOS with [110] transport may result in optimum density-of-states (DOS) and injection velocity, providing good ballistic performance topping Si or III-V nMOS [3].

Another important issue is the carrier transport model. To simulate the upper limit of current drivability, ballistic transport model has been widely used in many benchmarking studies [12, 13]. Even for extremely scaled devices ($L_G \lesssim 15$ nm), however, carrier scattering effects may be still significant [14]. While it is also critical to consider quantum transport effects such as tunneling in extremely scaled devices, it is very expensive numerically to incorporate scattering effects within a quantum transport simulation framework. In this study, to capture both effects of quantum transport and carrier scattering, we take a hybrid approach [6], by calculating the so-called "ballistic ratio" (*BR*) [15] from full-band Monte Carlo (MC) simulations [16, 17] and applying them as correction factors to the ballistic current-voltage (*I-V*) from atomistic quantum transport simulation [18-20] (**Fig. 4**).

While many benchmarking studies focus on the *I-V* characteristics of intrinsic devices, parasitic components such as S/D resistance (R_{SD}) may critically impact the actual performance. We have included realistic values of R_{SD} in most of our benchmarking studies, and we also showed that R_{SD} may also significantly depend on the S/D contact geometry due to the carrier scattering and momentum distribution effects [5], especially for light m^* materials such as III-V nMOS (**Fig. 5**). We also note that in addition to *I-V*'s, capacitance-voltage (*C-V*) and circuit performance metrics such as the effective drive current (I_{eff}) [21], switching energy (CV^2), and switching delay (CV/I) including relevant parasitics (such as R_{SD} and parasitic capacitance (C_{par})) and loading effects (gate or wire capacitance loading) are as important to correctly compare various CMOS combinations (homogeneous or heterogeneous) [4, 6] as shown in **Fig. 6**. We also note that for some channel materials such as Ge, we may have different S/D designs (e.g. N_{tip}'s) that provide optimum performance for the given operation target (high performance or low power).

Finally, while most of previous studies have been done at room temperature (T), we showed that the higher operating T's for circuits and systems [22] may have significant implications regarding CMOS benchmarking, especially for novel channel materials (**Fig. 7**) [7]. Due to different T-dependences of thermionic vs. tunneling leakages, for example, performance metrics such as the maximum supply voltage ($V_{DD,max}$) may increase at high T, providing improved I_{eff} in a wider range of V_{DD} while still satisfying Si-like leakage power conditions [7, 23].

While we have achieved significant benchmarking results for novel CMOS channel materials, there are still research gaps to be filled. First, while we introduced a hybrid approach [6] by combining results from two different simulation tools (quantum ballistic (fundamental) + MC (correction factors)) to capture both effects of quantum transport and carrier scattering, the research community may develop a more unified way (e.g. a new, numerically efficient approach to incorporate scattering into the quantum simulation framework) to accurately include those effects within a single, self-consistent simulation tool. Also, while we did consider some circuit aspects in our benchmarking (I_{eff}, CV^2, CV/I, operating T's), more in-depth simulations for the process and circuits may be done to analyze the material impact on the layout, fabrication, and system-level performance ("system-technology co-optimization"). This may be particularly important because novel CMOS channel materials may not only promise performance boost for individual transistors but also give integration challenges to the existing Si-based technology.

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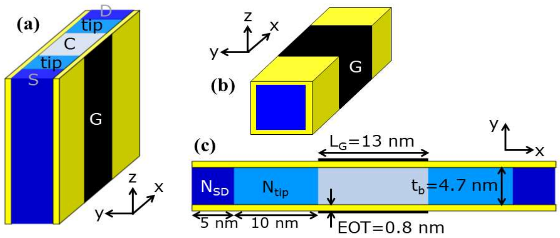

(d)

nMOS	Si	InAs	$In_{0.53}Ga_{0.47}As$	GaAs	Ge
N_{tip} (cm^{-3})	10^{20}	10^{19}	10^{19}	2×10^{19}	10^{19}, 2×10^{19}, 5×10^{19}

pMOS	Si	Ge
N_{tip} (cm^{-3})	10^{20}	10^{19}, 2×10^{19}, 5×10^{19}

x	y	z
[110]	[$\bar{1}$10]	[001]

Fig.1: Structures and parameters of L_G=13 nm model device (EOT: equivalent oxide thickness, t_b: body thickness, N_{SD}: S/D doping). (a) DG and (b) GAA NW MOSFETs. (c) Cross-sectional view. (d) n- and pMOS channel materials (with optimized N_{tip}'s) and crystal orientations (x, y, z).

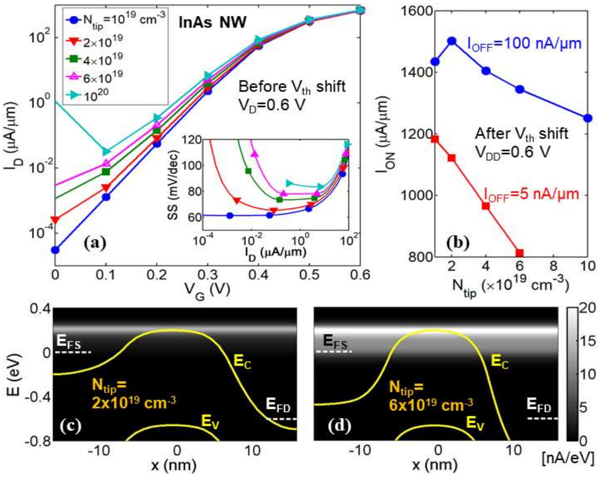

Fig. 2: Simulation results for (a) ballistic I_D vs. V_G (no R_{SD}) for various N_{tip}'s for InAs NW nMOS. (Inset) SS vs. I_D. (b) I_{ON} vs. N_{tip} for two I_{OFF} targets (V_{th}: threshold voltage, V_{DD}: supply voltage). (c)-(d) OFF-state (at V_G=0.2 V in (a)) energy-resolved current and band profiles for low and high N_{tip}'s (E_C/E_V: conduction/valence band, E_{FS}/E_{FD}: source/drain Fermi level).

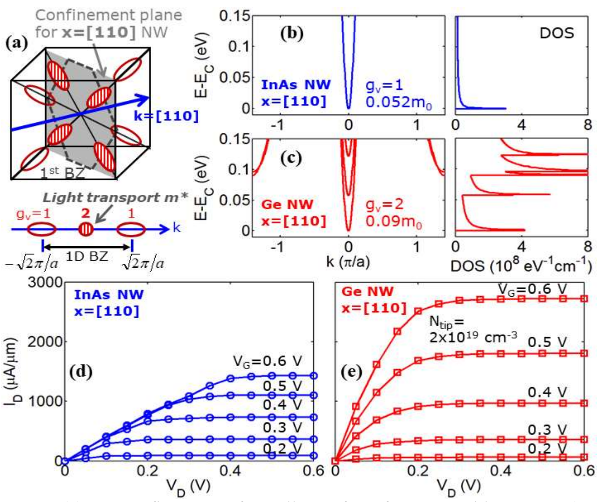

Fig. 3: (a) 2D confinement of L-valleys of Ge for NWs with x=[110] (g_v: valley degeneracy). 1D E-k and DOS of (b) InAs and (c) Ge NWs (g_v and m^* of the lowest band also shown, m_0: free electron mass). Simulation results for ballistic I_D vs. V_D (I_{OFF}=100 nA/μm, V_{DD}=0.6 V, no R_{SD}) for (d) InAs and (e) Ge NW nMOS with x=[110].

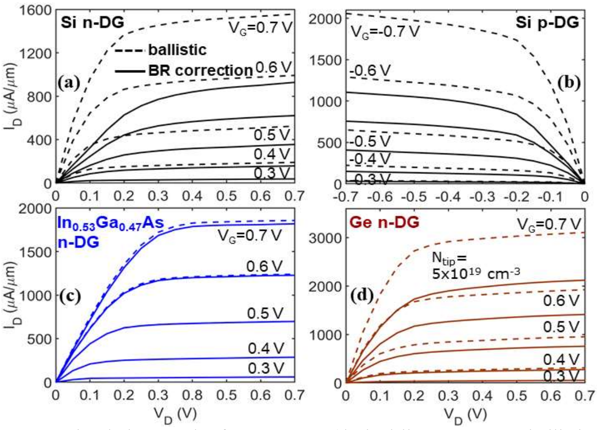

Fig. 4: Simulation results for I_D vs. V_D (dashed lines: quantum ballistic, solid lines: with BR correction, I_{OFF}=5 nA/μm, V_{DD}=0.7 V, no R_{SD}) for DG (a) Si nMOS, (b) Si pMOS, (c) $In_{0.53}Ga_{0.47}As$ nMOS, and (d) Ge nMOS.

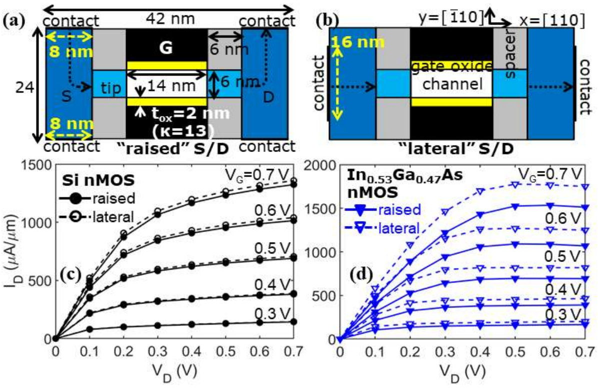

Fig. 5: Schematics of DG FETs with (a) "raised" and (b) "lateral" S/D contacts. MC simulation results for I_D vs. V_D (I_{OFF}=100 nA/μm, V_{DD}=0.7 V, contact resistivity=2×10^{-9} Ω-cm^2) for (c) Si and (d) $In_{0.53}Ga_{0.47}As$ nMOS.

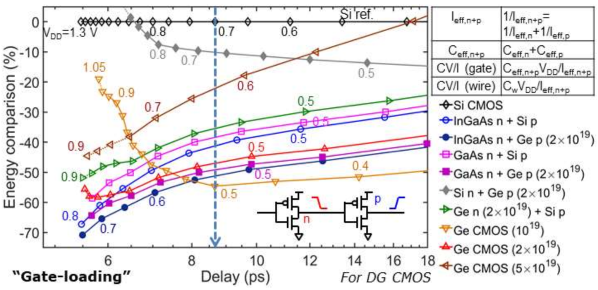

Fig. 6: Relative comparison of CV^2 vs. CV/I (gate capacitance loading) for various CMOS combinations against Si CMOS. R_{SD}=200 Ω-μm, C_{par}=0.6 fF/μm, and carrier scattering effects are all included. Formulations to calculate circuit metrics are also shown. Values in () are N_{tip} in cm^{-3} for Ge.

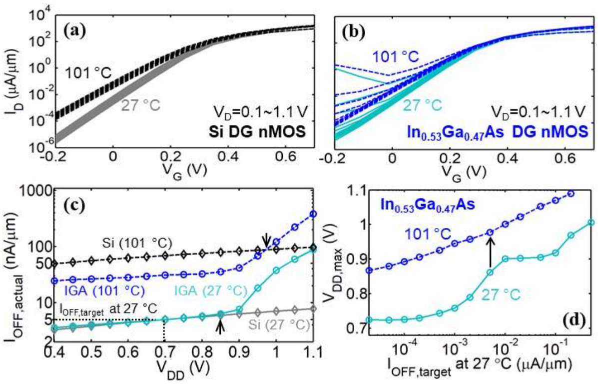

Fig. 7: Simulation results for (a)-(b) I_D vs. V_G, (c) $I_{OFF,actual}$ (I_D at V_G=0 V, V_D=V_{DD}) vs. V_{DD}, and (d) $V_{DD,max}$ vs. $I_{OFF,target}$ (I_{OFF} target at 27 °C and V_{DD}=0.7 V) at **27 °C vs. 101 °C** for Si and $In_{0.53}Ga_{0.47}As$ (IGA) DG nMOS.