Effects of Thin Dipole Layer in Silicon Tunnel Field Effect Transistors

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Tunnel FETs (TFETs) are a promising device for low-power integrated circuits owing to its low operation voltage and steep sub-threshold swing. However, Si TFETs have limitations in terms of on-state current (I_{on}) and on-off ratio due to large band gap and heavy tunneling effective mass [1]. One of the approaches to overcome these shortcomings is to devise TFETs with broken/staggered band gap by forming heterostructures. The band offset of heterojunction III-V materials which have polar interface can be controllable by inserting group-IV ultra-thin layer [2]. Similarly, band alignments can be engineered by inserting a dipole layer in an otherwise homogeneous structure. In this study, we have constructed silicon ultra-thin body (UTB) double-gate (DG) TFETs in the (110)/[001] orientation with III-V ultra-thin layers inserted to create band offset between source and channel region. The density functional theory (DFT) is employed and full quantum transport simulations are performed.

The DFT Hamiltonians are extracted by SIESTA code and all the atomic structures are fully relaxed. The size of the Hamiltonians is reduced by reduced basis transform method for efficient transport simulation [3]. To calculate the current, non-equilibrium Green's function and Poisson's equation are self-consistently solved.

The insertion of the III-V layer in the silicon channel forms dipoles and the electric field induced by dipoles shift the electrostatic potential, resulting in a staggered gap (Fig.3). As a consequence, the band-to-band tunneling distance can be effectively reduced, so I_{on} can be increased by a few orders of magnitude compared to Si homojunction TFET without dipole layer (Fig. 4, 5). Furthermore, we expect that silicon's large band gap will effectively suppress the ambipolar behavior, which is an issue in TFETs.

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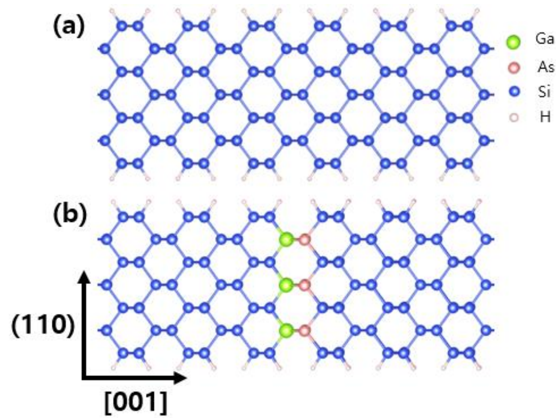

Fig.1: Atomic structures of (a) Si homojunction and (b) insertion of III-V (GaAs) dipole layer.

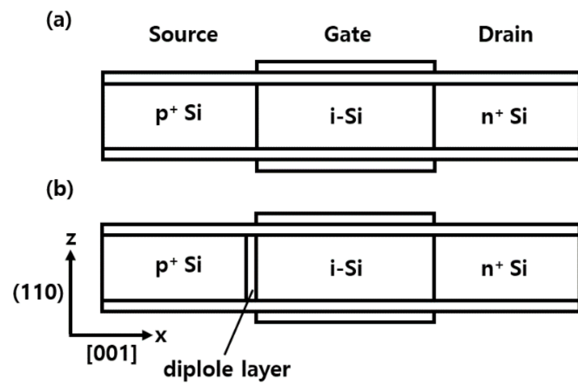

Fig.2: Schematics of DG (a) Si homojunction TFET and (b) insertion of dipole layer.

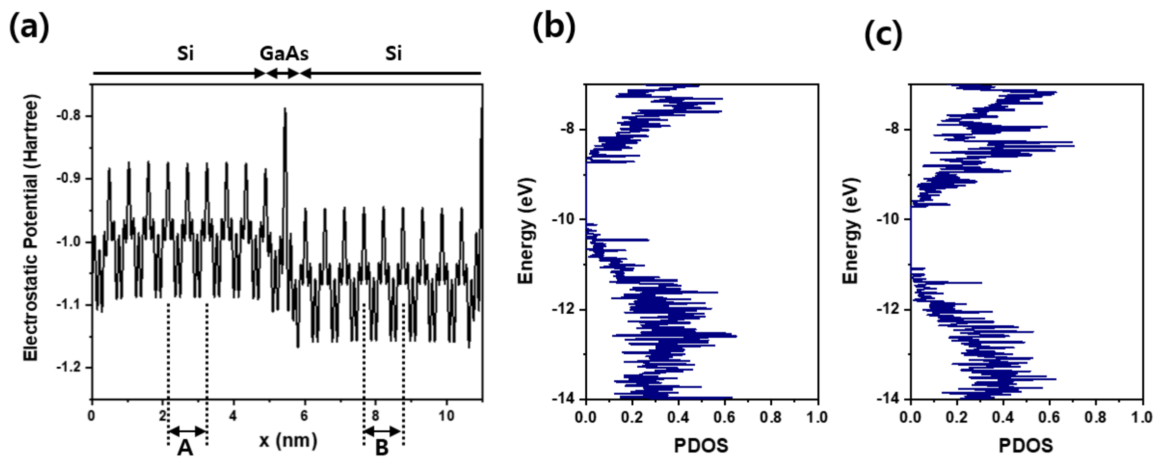

Fig.3: (a) Electrostatic potential and PDOS of (b) left side (region A of (a)) and (c) right side (region B of (a)) of the dipole layer. The UTB has a body thickness of 2nm.

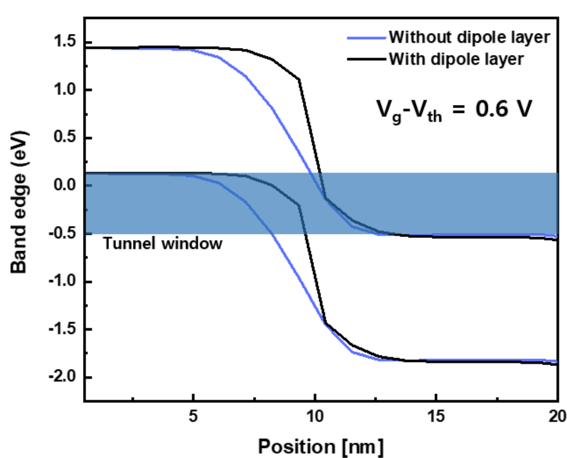

Fig.4: Band diagrams at on-state ($V_g - V_{th} = 0.6$ V) of TFETs with and without GaAs dipole layer. $V_d = 0.5$ V. $V_{th} = V_g$ @ $I_{ds} = 10^{-5}$ μA/μm.

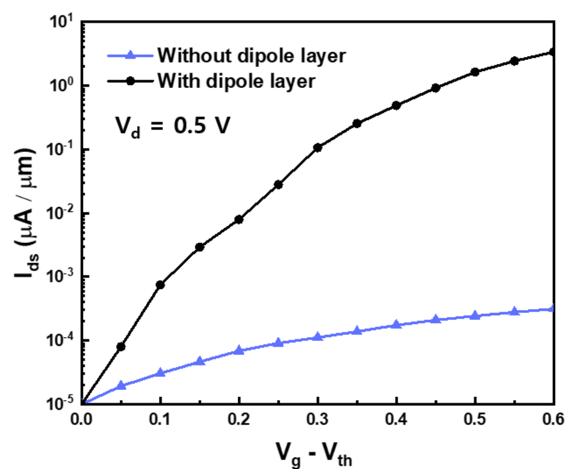

Fig.5: Transfer IV characteristics of TFETs with and without GaAs dipole layer.

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