Interfacial Trap Effects in InAs Gate-all-around Nanowire Tunnel Field-Effect Transistors: First-Principles-Based Approach

Hyeongu Lee[1], Yucheol Cho[1], Seonghyeok Jeon[1], and Mincheol Shin*[1]

[1] *School of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 34141, Republic of Korea*
mshin@kaist.ac.kr

III-V materials have been actively adopted for the channel material to improve on-current of tunnel field-effect transistors (TFETs). But, one of the issues in practical III-V channel TFETs is the possible presence of interfacial traps between III-V channel and dielectric oxide [1]. A recent first-principles study reported that the dangling bond and anti-site traps can induce the bandgap states which critically affect the TFET performance [2]. However, the effects of these traps using full quantum transport simulation has not yet been investigated. To correctly understand the trap effects and provide practical guidelines for better TFET performance, it is essential to rigorously capture the impact of trapped charges and trap-assisted tunneling (TAT). In this work, we investigated the effects of the traps, Arsenic dangling bond (As_{DB}) and Arsenic anti-site (As_{In}) traps, in InAs gate-all-around nanowire TFETs, using the trap Hamiltonian obtained from the first-principles calculations. The transport properties were treated by nonequilibrium Green's function including the phonon scattering with self-consistent Born approximation. We have focused on the effects of the gate length (L_G) and the trap position (x_T).

The schematic of the simulated device are shown in Fig. 1. Local density of state and current spectrums are shown in Fig. 2, where the As_{DB} trap is located above the valence band edge and the As_{In} trap is at the midgap. Fig. 3 shows the transfer characteristics for L_G = 7, 10, 14, and 17 nm. The traps mainly affect the subthreshold properties, and the impact becomes more significant as L_G decreases. The average SS (SS_{avg}) and I_{ON}/I_{OFF} are depicted in Fig. 4 which reveals that the As_{In} trap is the most detrimental trap for deep L_G scaling. Fig. 5 shows that the degradation by the As_{In} trap is caused by the trap charges (hole) which effectively block the gate electric field so that the TAT leakage current continues to take place. The effect of x_T is shown in Fig. 6 which shows that even a single trap can have significant effects on the reliability and the traps located near source-side are more responsible than the traps near drain-side.

Acknowledgments
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[2] G. Greene-Diniz et al, J. Appl. Phys., **121**, 075703 (2017)

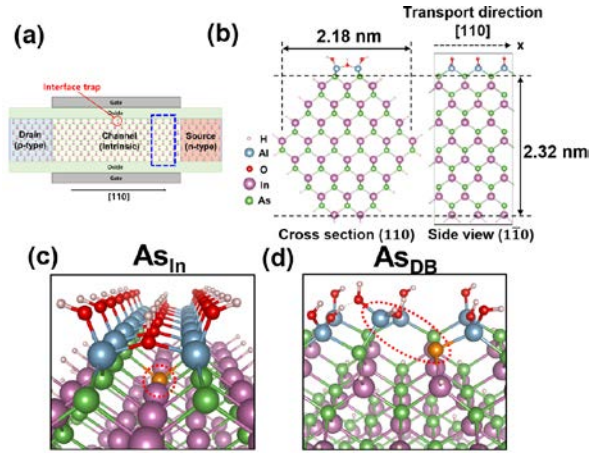

Fig. 1. (a) Schematic of InAs TFET with [110] transport direction. The dashed box indicates the defect-free supercell for density functional theory calculation. Relaxed atomistic structures of (b) the defect-free supercell and the supercell with (c) As_{In} trap and (d) As_{DB} trap. The traps are indicated by red circle.

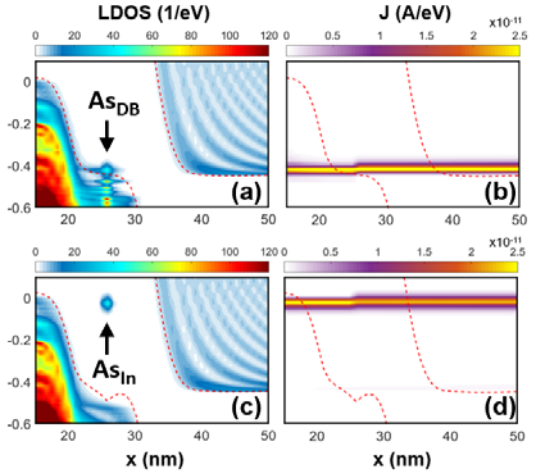

Fig. 2. Local density of states (LDOS) and current spectrum (J) for LG = 10 nm. LDOS of (a) As_{DB} trap and (c) As_{In} trap. J of (b) As_{DB} trap and (d) As_{In} trap. The drain Fermi level is set to zero.

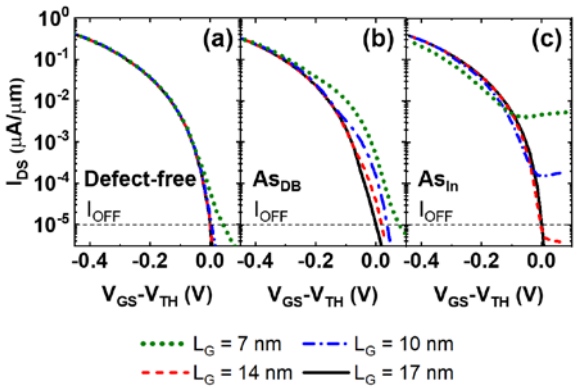

Fig. 3. Transfer characteristics of InAs TFETs (a) without the trap, (b) with As_{DB} trap, and (c) with As_{In} trap. The gate voltage is shifted by the threshold voltage of the device with L_G = 17 nm.

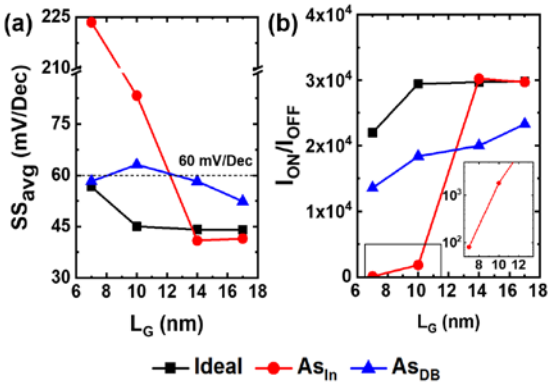

Fig. 4. (a) SS_{avg} and (b) I_{ON}/I_{OFF} as functions of L_G. SS_{avg} is calculated over the three orders of magnitude of the drain current from I_{OFF} = 10^{-5} A/m.

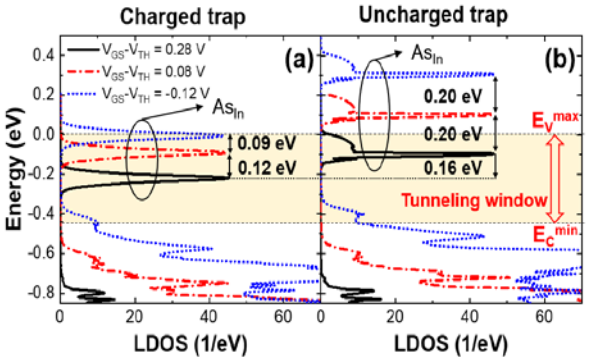

Fig 5. LDOS of the transport unit cell where the trap is located: (a) with the trap being charged and (b) without the trap being charged. E_C^{min} and E_V^{max} are the conduction band minima and valence band maxima throughout the device, respectively. The tunneling window is shaded.

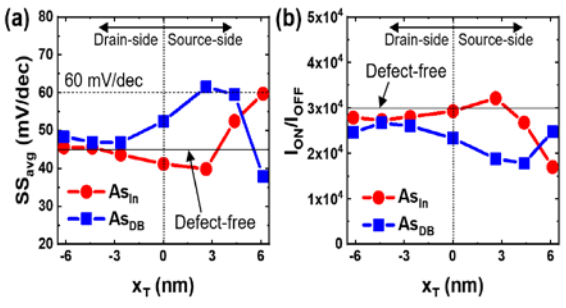

Fig 6. (a) SS_{avg} and (b) I_{ON}/I_{OFF} as a function of x_T. The gate length is 17 nm. The dashed lines indicate the performance of TFETs without trap. x_T is measured from the center of the channel.