

## Random Telegraph Noise of Gate-All-Around Silicon Nanowire MOSFETs Induced by Single Charge Trap

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We for the first time study random telegraph noise (RTN) of cylindrical shape gate-all-around silicon nanowire (GAA Si NW) metal-oxide-semiconductor field effect transistors (MOSFETs) with spacer induced by acceptor-type single-charge trap for sub-7-nm technologies. For GAA NW MOSFETs, the trap position dependence on the RTN magnitude ( $(\Delta I_D/I_D) \times 100\%$ ) in channel is observed. The impact of RTN located middle of the channel is significant. The reduction of on-state current of the explored device with and without spacer are 9.3% and the gate capacitance can be reduced up to 18.56%. Gate-all-around silicon nanowire MOSFET is a promising device for sub-7-nm technology nodes owing to its ultimately electrostatic controllability and good short channel effects (SCE) immunity [1-3]. In this work, we study the transfer characteristic ( $I_D-V_G$ ) and gate capacitance ( $C-V$ ) of device with spacer. Random telegraph noise influenced by acceptor-type single charge trap (SCT) presenting at different positions along the channel [4-6] between silicon and silicon dioxide for N-type GAA Si NW MOSFET devices by using an experimentally validated 3D device simulation under the similar parameters settings. The magnitude of RTN induced by cylindrical-type SCT along the channel is estimated for the nominal GAA Si NW MOSFET and the device with spacer. At the drain due to band-to-band tunneling the reduction of RTN is caused. By extracting SCE parameters, we discuss characteristic variability induced by SCT. We observe that the magnitude of RTN is high at the SCT middle (i.e., B of Fig. 1(a)) position to source and drain. Figures 1(c) and (d) illustrate the simulated structures for nominal and with spacer GAA Si NW MOSFETs devices. Figures 1(a) and (b) show the positions of SCTs and cross-section view of the channel respectively. The density of interface trap ( $D_{IT}$ ) is greater than  $10^{12} \text{ cm}^{-2}$ . This simulation is examined by solving 3D quantum-mechanically corrected transport model which is valid by nonequilibrium green function (NEGF) [1]. We express the simulation results, evaluate  $I_D-V_G$  electrical characteristics variability due to spacer is shown in Fig. 2; here, the  $\text{SiO}_2$  acts as low- $\epsilon$  dielectric material. The spacer acts like capacitor. The reduction of on-state current of the explored device with and without spacer are 9.3%. Similarly, for the  $C-V$  analysis, the capacitance varies largely due to dielectric charging and discharging, which we can clearly observe from Fig. 3. However, for realistic nano-CMOS technologies, the dependence of RTN not only on device geometry but also the trap's location and energy. Figures 4 and 5 illustrate the amplitude of the RTN in the presence of SCT (by calculating the deviation  $\Delta I_D/I_D \times 100\%$ .) due to trapping/de-trapping in different location for nominal device and the device with spacer, respectively. The amplitude of RTN decreases with increasing  $V_G$  due to the low charge carriers. Finally, The RTN amplitude is large when SCT is placed at the position B. As listed in Tab. 1, we compare the magnitudes of RTN for the nominal GAA Si NW MOSFET and the device with spacer, respectively, at the off-state for both doped and undoped channels. Notably, for the device with spacer and undoped channel, the large magnitude of RTN is observed for the trap at position B. In summary, we have investigated the SCT induced RTN; and, for device with spacer and undoped channel, the magnitude of RTN is high when the trap is located at middle of the channel.

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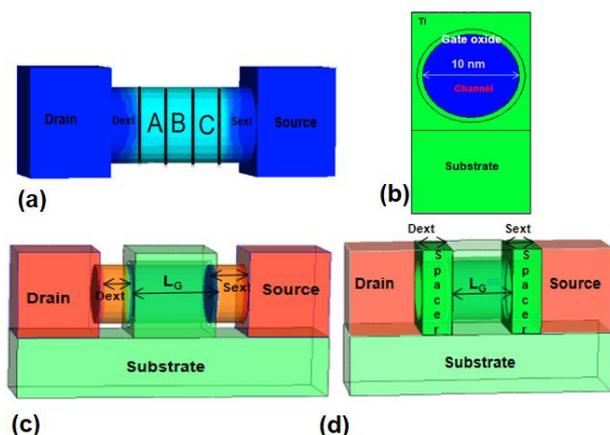


Fig. 1: (a) The single charge trap is located at different position along the channel on the interface of Si/SiO<sub>2</sub>. (b) The cross-sectional view at the middle of the channel. (c) and (d) are the 3D simulated structures of the GAA NW MOSFET without/with spacer.

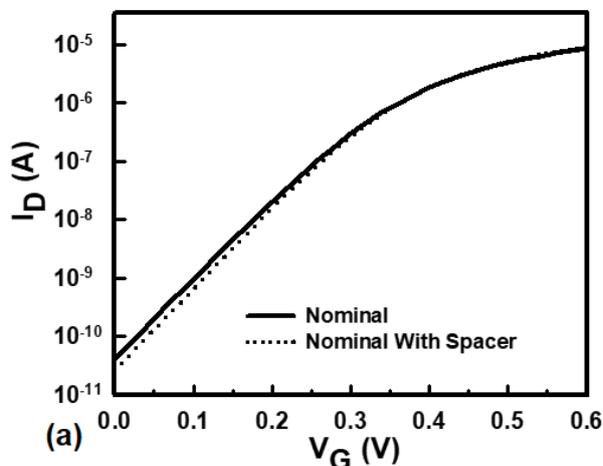


Fig. 2:  $I_D$ - $V_G$  plots of electrical characteristics comparison (i.e., nominal device (solid line) and device with spacer (dot)) under the biasing of  $V_D=0.6$  V and the same settings of parameters for both devices.

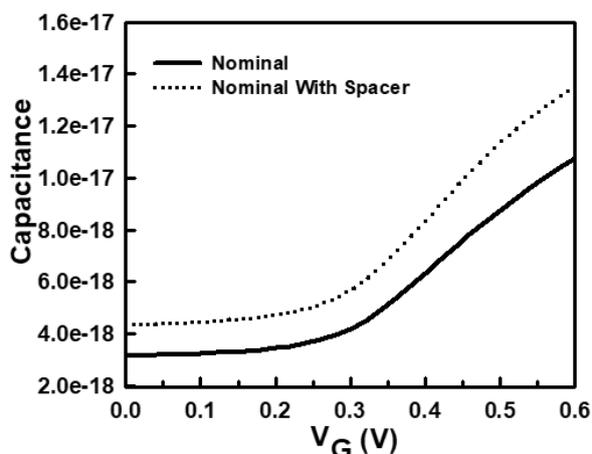


Fig. 3: C-V comparison of the simulated devices (i.e., nominal device (solid line) and device with spacer (dot)) under the similar parameters and biasing condition of  $V_D=0.6$  V.

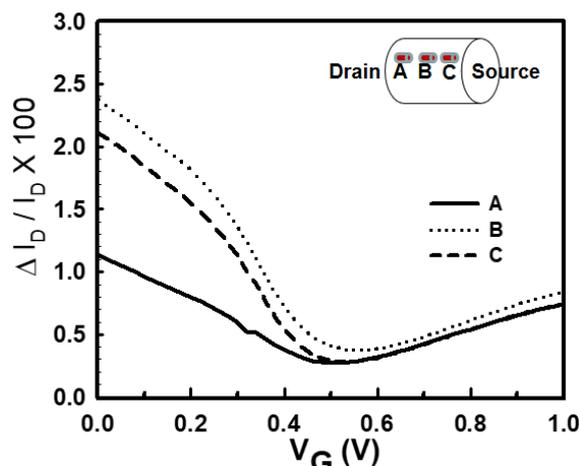


Fig. 4: The comparison of calculated magnitude (%) of the random telegraph noise in the presence of the acceptor-type single charge trap at different locations in the channel for nominal GAA NW MOSFET under  $V_D=0.01$  V.

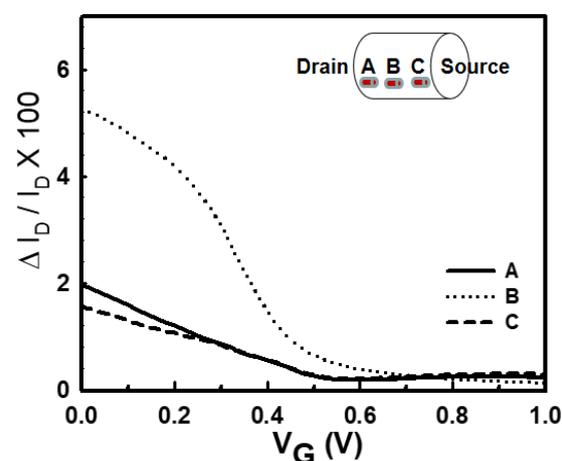


Fig. 5 The comparison of calculated magnitude (%) of the random telegraph noise in the presence of the acceptor-type single charge trap at different locations in the channel for with spacer GAA NW MOSFET under  $V_D=0.01$  V.

Tab. 1: List of calculated magnitudes of RTN (%) comparison in the presence of the acceptor-type SCT placed in different position along the channel for the nominal and with spacer GAA NW MOSFETs under the doped and undoped channel, with similar biasing conditions and device settings.

Type of Device	SCT Position		
	A	B	C
Without spacer & doped channel	1.095	2.310	2.280
Without spacer & undoped channel	1.290	2.390	2.380
Spacer & doped channel	2.000	5.200	1.560
Spacer & undoped channel	2.200	5.300	1.620