# Quantum Transport Simulations of Gate-all-around Nanowire pFETs with Arbitrary Shaped Cross-section in the Presence of Hole-phonon Interaction

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Gate-all-around nanowire field-effect-transistors (GAA NW FETs) with the excellent electrostatic integrity are considered as a promising candidate for sub-10 nm CMOS technology. In order to assess the true potential of the devices, it is essential to capture the phonon scattering effects together with the quantum effects such as quantum confinement and tunneling. Although simulations of realistically sized devices including these effects have been extensively conducted for n-type transistors, those for p-type transistors are quite lacking. In this work, we have developed an efficient quantum transport simulator for p-type GAA NW FETs, which has the capabilities to include the hole-phonon scattering and handle arbitrary shaped cross-section. We have used the multiband k·p models to describe the valence bands. To faithfully represent an arbitrary shaped cross-section of NW, we have employed the finite element method (FEM) for a three-dimensional (3D) discretization of the k·p Hamiltonians and the Poisson equation as shown in Fig. 1. The hole-phonon interaction has been treated in the framework of the nonequilibrium Green's function (NEGF) method through the self-consistent Born approximation (SCBA) and assumed to be local. For efficient NEGF simulations, the size of the $k \cdot p$ Hamiltonians is reduced using the mode space approach [1] where the Bloch modes are sampled in energy and k space. We have developed an efficient scheme to calculate the hole-phonon self energy in the mode space which greatly reduce the computational cost of SCBA. See Fig. 2. for the flowchart. For validation of the simulator, we have compared the low-field hole mobilities of silicon NWs with those of the tight-binding (TB) full band simulations [2] and found that our results agree well with the TB results as shown in Fig. 3. Also, the inelastic scattering effects are seem to be captured correctly in Fig. 4. As an application, we have studied the impacts of the cross-section aspect ratio on the device performance of silicon pFET along the [110] transport direction in Fig. 5. Our simulator can be used as a practical tool for design and optimization of GAA NW pFETs.

[1] M. Shin et al., J. Appl. Phys, **119**, 154505 (2016).

[2] M. Luiser et al., IEDM Tech. Dig., pp. 8.6.1-8.6.4 (2010).

[3] A. Ziegler et al., SISPAD, pp. 25-28, (2017).

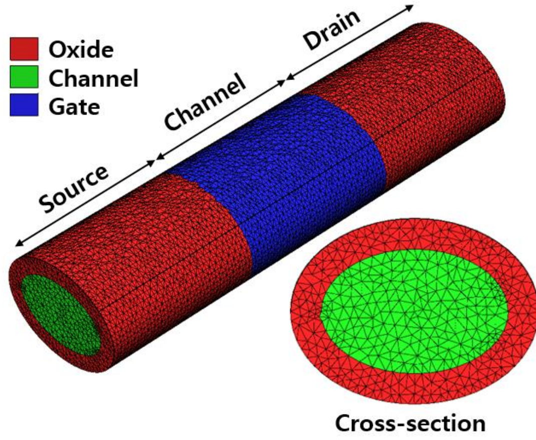


*Fig.1: Schematic of GAA nanowire and the cross-section with the finite element mesh configuration.*

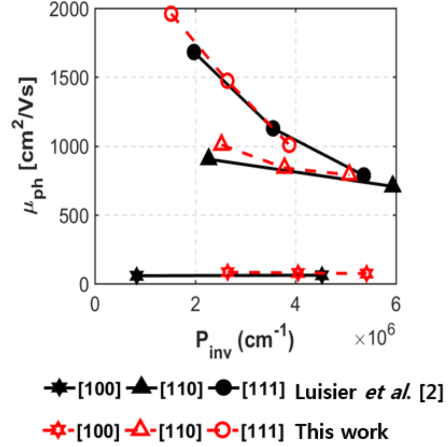


*Fig.3: The low-field hole mobility $\mu_{ph}$ of a silicon nanowire as a function of hole inversion density $P_{inv}$ at the top of the barrier at $V_{ds} = 10^{-4}$ V. The diameter of silicon nanowire is 3.0 nm and the source and drain lengths are 10.0 nm. The scaling parameters of the deformation potentials for phonon confinement effects were taken from Ref. [3].*

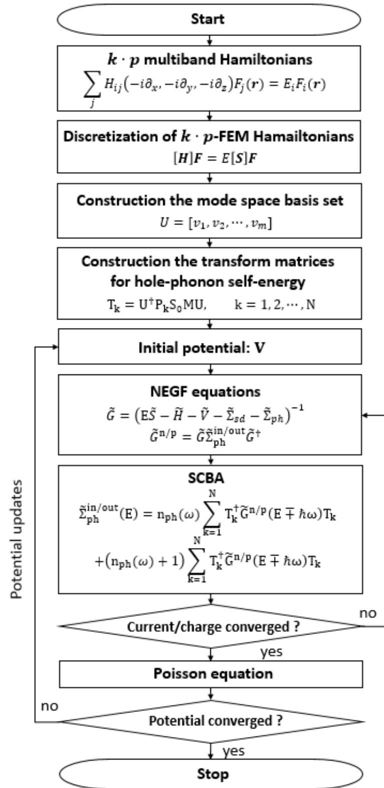


*Fig.2: Flowchart of the overall simulation procedure. m is the number of modes and N is the number of the FEM nodes of the periodic layer. $P_k$ is the orthogonal projection onto the subspace spanned by the multiband basis vectors of the k-th FEM node. $S_0$ is the overlap matrix and $n_{ph}(\omega)$ is the Bose-Einstein distribution of the phonon with frequency $\omega$.*

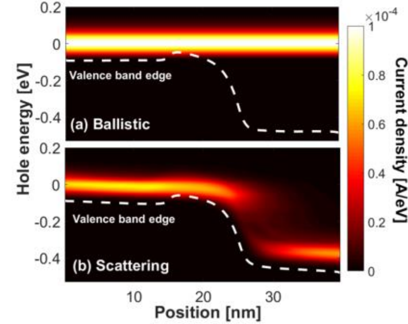


*Fig.4: Current spectrum of a silicon NW pFET in (a) ballistic transport and (b) scattering transport at $V_{GS} = -0.4$ V and $V_{DD}$ = 0.4 V. The NW diameter is 5.0 nm and the source, channel, and drain lengths are 15.0 nm, 10.0 nm, and 15.0 nm respectively.*

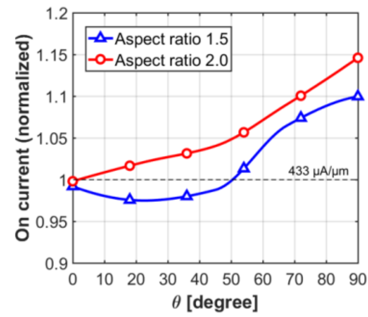


*Fig.5: On-current of silicon NW pFETs as a function of $\theta$ where $\theta$ is the angle between the major axis of NW and (001) plane. The transport direction is <110>. The source-drain voltage is -0.4 V and the driving voltage is 0.4 V. The dashed line is the on-current of the device with the aspect ratio of 1.0. All devices have the same cross-section area as that of NW with the diameter of 5.0 nm.*