3D Schrödinger Equation Quantum Corrected Monte Carlo and Drift Diffusion Simulations of Stacked Nanosheet Gate-All-Around Transistor

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Nanosheet silicon channel transistors laterally stacked in pillars are one of the promising solutions for 5~nm technology nodes and beyond for logic applications [1]. The nanosheet transistor architecture with a wrap-around-gate (WAG) contact can deliver the same excellent electrostatic integrity as SOI FinFETs [2] or nanowire GAA FETs [3] while can deliver a larger on-current required by ITRS 2.0 prescriptions [4] and be fabricated with fewer deviations from the already established FinFET manufacturing. The most importantly, the fabrication of nanosheet FETs can overcome many of patterning challenges present in a nanoscale fabrication of stacked nanowires and closely stacked FinFETs [1].

In this work, we employ in-house 3D finite element (FE) Monte Carlo (MC) and drift-diffusion (DD) device simulation tools with quantum corrections to accurately model Si nanosheet transistors with the WAG illustrated in Figs. 1 and 2. The quantum corrections in the 3D FE MC simulations [5] use solutions of 2D Schrödinger equation (SchE) [6] assuming longitudinal and transverse electron effective masses in Si and wavefunctions penetrating into a surrounding high-κ dielectric layer [7,8]. The SchE is solved on 2D slices across the channel with a non-uniform distribution dependent on a gradient of electron density along the channel. The 3D FE MC simulations use Fermi-Dirac statistics in electron scattering with ionised impurities via static screening with a self-consistently calculated Fermi energy and electron temperature in real space of a device [8,9]. Two types of quantum corrections can be included in the 3D DD simulations: (i) 3D FE density gradient (DG) [10] which require calibration parameters and (ii) 2D SchE on slices along the channel as in the 3D FE MC simulations. The quantum corrections using eigenstates of the 2D SchE, $\psi_i(y,z;E_i)$, and eigenenergies, E_i, have been incorporated into the 3D FE DD simulations for this work. A quantum-mechanical electron density in Boltzmann approximation (6 equivalent valleys) can be obtained as [7]:

$$n_Q(y,z) = 6\frac{\sqrt{2\pi m^* k_B T}}{\pi\hbar} \sum_i |\psi_i(y,z;E_i)|^2 \exp\left[\frac{E_{F_n} - E_i}{k_B T}\right]$$

where k_B is the Boltzmann constant, T is the electron temperature, and E_{F_n} is the electron quasi-Fermi level. The 2D quantum density, $n_Q(y,z)$, is interpolated using spline functions to a 3D device density domain, $n_Q(\boldsymbol{r})$. A quantum correction potential, $V_{qc}(\boldsymbol{r})$, reads [6]:

$$V_Q(\boldsymbol{r}) = k_B T \log\left[n_Q(\boldsymbol{r})\right] - V(\boldsymbol{r}) - k_B T \log\left[n_i^{\text{eff}}(\boldsymbol{r})\right]$$

where $V(\boldsymbol{r})$ is the potential energy, and $n_i^{\text{eff}}(\boldsymbol{r})$ is the effective intrinsic concentration.

A schematic cross-section of a stack with three Si nanosheet transistors with the WAG is illustrated in Fig. 1 which closely follows the 12 nm gate length nanosheet transistor reported in Ref. [1] by IBM, Samsung, and Global Foundries consortium. Fig. 2 shows a cross-section of three nanosheet transistors made of the outer metal gate and inner polysilicon gate closely surrounding a nanosheet *p*-type doped Si body covered with a high-κ dielectric layer [1]. The device has a Si channel with a 50 nm width and a height of 5 nm surrounded by a high-κ dielectric layer of a thickness of 1 nm and a dielectric constant of 3.9. We have then studied a performance of the nanosheet transistors when their width would be scaled down in order to reduce area of the CMOS to acquire a large transistor density on a chip. Fig. 3 illustrates quantum corrected electrostatic potential in cross-sections of a nanosheet FET scaled from a width of 50 nm to 30 nm, 10 nm, and 5 nm.

The comparison of the I_D-V_G characteristics obtained from 3D FE DD and MC simulations with experimental data are presented in Figs. 4-5 at a low drain bias of 0.0 V and a high drain bias of 0.7 V, respectively. The source/drain *n*-type doping has been reverse engineered using a Gaussian doping profile with a peak doping of 5×10^{19} cm^{-3} and a spread σ_x of 3.45 nm. The DD uses Caughey-Thomas doping dependent low-field electron mobility model combined with perpendicular (critical electric field) and lateral (saturation velocity) electric field models with a calibrated low-field mobility of 50.24 cm^2/Vs, a saturation velocity of 1.8×10^6 cm/s (1.7×10^7 cm/s), and a critical electric field of 1×10^6 V/cm (1×10^9 V/cm) at V_D = 0.05 V (V_D = 0.7 V), respectively. The interface roughness which plays a crucial role in multi-gate transistors at a high drain bias [5] assumes a RMS height of 1.5 nm and a correlation length of 1.7 nm. The DG quantum corrected DD exhibits only 2% difference between more accurate SchE quantum corrections used in DD and MC simulations while a difference between the SchE quantum corrected DD and MC simulations is nearly negligible. Figs. 6-8 show I_D-V_G characteristics at a high drain bias of 0.7 V when the width of Si nanosheet is reduced from 50 nm to 30 nm, 10 nm, and 5 nm. The respective reduction in the drain current normalised to a nanosheet circumference obtained from the 3D MC will be 10.7%, 34.2%, and 48.7% making the nanosheet width scaling below 30 nm meaningless.

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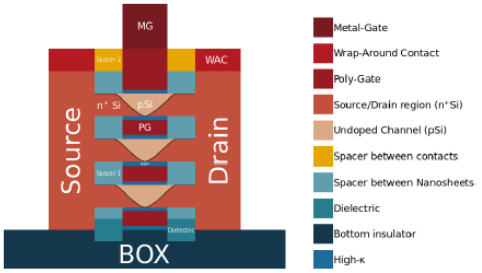

Fig. 1: Schematic cross-section of a typical Si nanosheet multi-gate transistor with three integrated nanosheets [1].

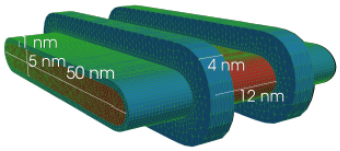

Fig. 2: A finite element mesh to accurately describe one nanosheet wrap-around channel multi-gate transistor.

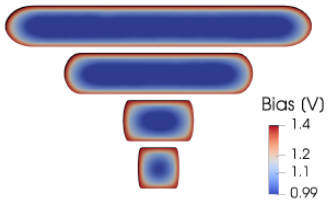

Fig. 3: Potential cross-section in the middle of the gate for nanosheet FETs with widths of 50, 30, 10 and 5 nm from top to bottom, respectively, at $V_D = 0.7$ V and $V_G = 1.0$ V.

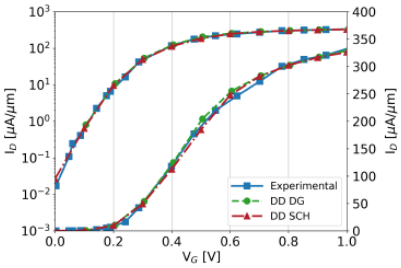

Fig. 4: I_D-V_G characteristics at V_D=0.05 V for the 12 nm gate length wrap-around channel nanosheet multi-gate FET comparing drift-diffusion simulations using density gradient (DD DG) and SchE (DD SCH) quantum corrections against experimental measurements [1].

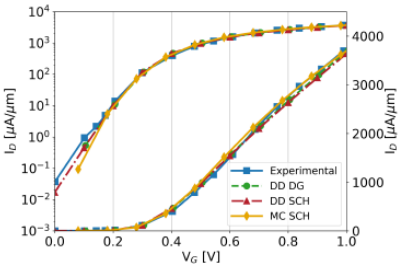

Fig. 5: I_D-V_G characteristics at V_D=0.7 V for the 12 nm gate length wrap-around channel nanosheet multi-gate FET comparing drift-diffusion simulations using density gradient (DD DG) and SchE (DD SCH) quantum corrections, and SchE quantum corrected Monte Carlo simulations (MC SCH) against experimental measurements [1].

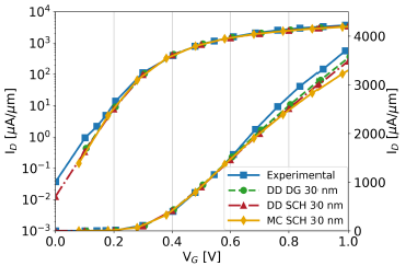

Fig. 6: I_D-V_G characteristics at V_D=0.7 V for the 12 nm gate length nanosheet FET obtained from Schrödinger Equation quantum corrected Monte Carlo simulations (MC SCH) with a nanosheet width reduced to 30 nm. The results from quantum corrected drift-diffusion simulations (DD DG and DD SCH) are for comparison.

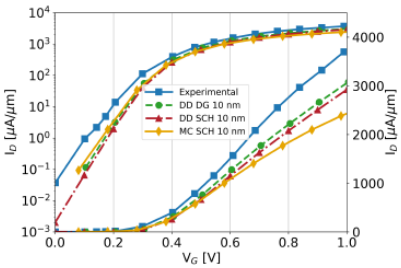

Fig. 7: I_D-V_G characteristics at V_D=0.7 V for the 12 nm gate length nanosheet FET obtained from SchE quantum corrected Monte Carlo simulations (MC SCH) with a nanosheet width reduced to 10 nm. The results from quantum corrected drift-diffusion simulations (DD DG and DD SCH) are for comparison.

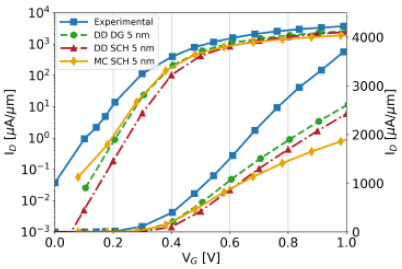

Fig. 8: I_D-V_G characteristics at V_D=0.7 V for the 12 nm gate length nanosheet FET obtained from SchE quantum corrected Monte Carlo simulations (MC SCH) with a nanosheet width reduced to 5 nm. The results from quantum corrected drift-diffusion simulations (DD DG and DD SCH) are for comparison.

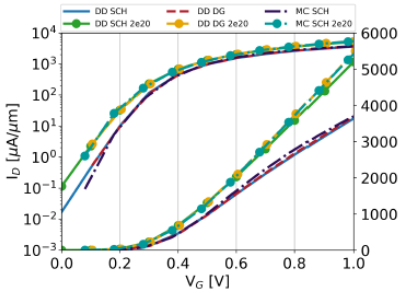

Fig. 9: I_D-V_G characteristics at V_D=0.7 V for the same nanosheet FET with a nanosheet width of 50 nm but assuming *n*-type S/D of 2×10^{20}cm^{-3} obtained from SchE quantum corrected MC simulations (MC SCH). The results from quantum corrected DD simulations (DD DG and DD SCH) are for comparison.