TCAD Based Performance Evaluation on Si NWTs

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All Gate Around (AGA) silicon (Si) Nanowire Transistors (NWTs) have the ultimate electrostatic integrity and are considered as suitable candidates for 5nm CMOS technology and beyond [1]. Their operation is governed by strong quantum confinement effects and non-equilibrium quasi-ballistic transport. Therefore the Ensemble Monte Carlo transport simulations are the best vehicle for studying of their performance. Here we report a comprehensive EMC simulation study of NWTs suitable for 5nm CMOS technology generation. The quantum confinement effects are properly taken into account in the MC simulations using the effective quantum potential approach based both on the solution of the Poisson-Schrodinger (PS) equation and on the Density Gradient (DG) algorithm. The impact of the NWT cross sectional shape, channel orientation and strain are taken into consideration. The simulations are carried out with GARAND (Synopsys). Due to the heavy computational requirements only single NWT are simulated using the EMC approach. Multi-channel NWTs with complex contact arrangements are simulated using the Drift Diffusion (DD) approach meticulously calibrated to the EMC simulations. The study concludes with the optimal NWT design, meeting the requirements for the 5nm CMOS technology and beyond. The DD simulations are also used to evaluate the statistical variability in the multichannel NWTs.

The cross section of the single channel Si NWT used in the EMC simulations is illustrated in Fig.1. The quantum mechanical charge distribution in the cross section of the simulated NWTs with different shape is illustrated in Fig. 2. Fig. 3 presents the dependence of the mobile charge in the NWT channel as a function of the gate bias. A very interesting observation is that the largest amount of mobile charge is available in NWTs with elliptical cross section obeying the Golden Rule (GR) ratio as illustrated in Fig. 4. The EMC simulations also confirm that the GR NWT has the best drive current performance as illustrated in Fig. 5. The simulation domain for the multi-channel Si NWTs used in the DD simulations calibrated in respect of the EMC simulations are illustrated in Fig. 6. Results for the performance of the multi-channels NWTs will be presented at the conferences together with a comprehensive study of the corresponding variability.

[1] *J.-P. Colinge, FinFETs and Other Multi-Gate Transistors*. Boston, MA: Springer US, 2008

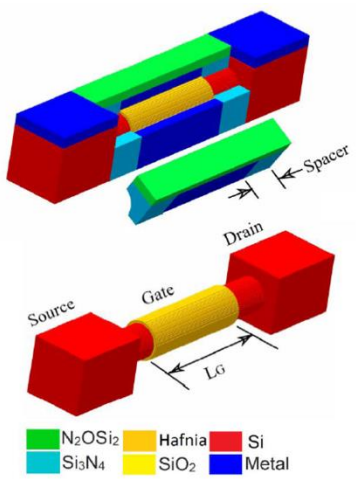

Fig.1: Cross section of the single channel Si NWT used in the EMC simulations.

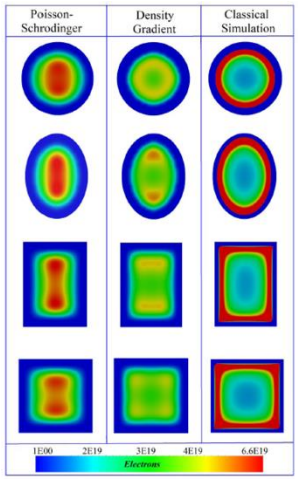

Fig2: quantum mechanical charge distribution in the cross section of the simulated NWTs with different shape.

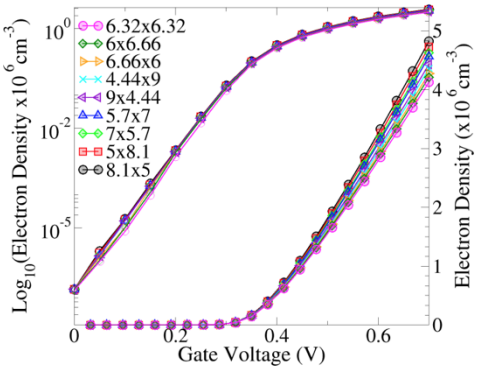

Fig.3: dependence of the mobile charge in the NWT channel as a function of the gate bias.

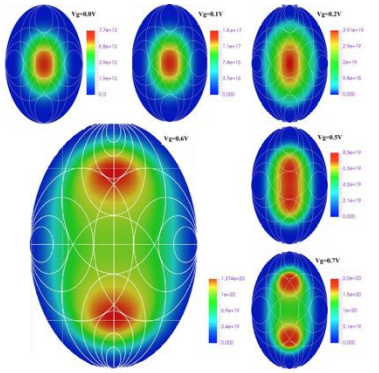

Fig.4 Normalized current as a function of the position x relative to silicon, for p=1, $\Gamma_N=\Gamma_0 \exp(-x/d)$, $\Gamma_F=\Gamma_0 \exp(-(d-x)/d)$, $T_2=T_1$, $\omega_L T_2 = \Gamma_0 T_2 = 10$,

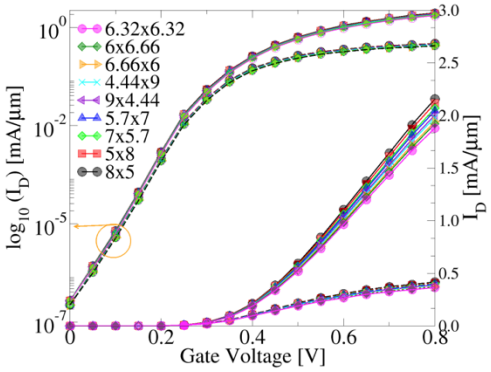

Fig.5: Current as a function the gate voltage for NWT with different cross section obtained from the EMC simulations.

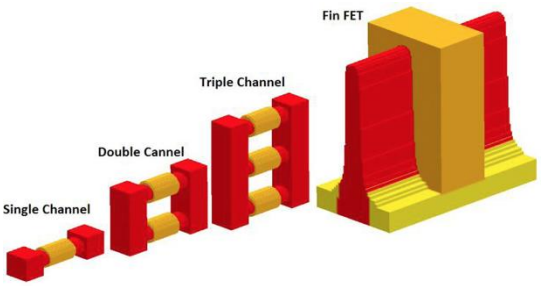

Fig.6: DD simulation domain for evaluating the performance of multichannel NWTs.