Multi-Scale Thermal and Electrical Modeling of CMOS Devices and Circuits

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This simulation work explores the thermal effects on electrical characteristics of CMOS devices and circuits using a multiscale dual-carrier approach. Simulating both electron and hole transport along with carrier-phonon interactions and thermal transport allows for the study of complementary logic circuits with device level accuracy regarding electrical performance and thermal effects. The electrical model is comprised of an ensemble Monte Carlo solution of the Boltzmann Transport Equation, coupled with a Poisson solver [1]; parametric iteration ensures current and voltage continuity in the circuit. The thermal model solves for carrier-phonon interactions in the device and phonon-phonon transport in interconnects [2]. This allows for modeling device behavior, analyzing circuit performance, and understanding thermal effects.

The electro-thermal approach is an improvement over de-coupled device simulators [3]. While initially developed to study individual NMOS devices, expanding this method for simulation of multiple NMOS devices in a tandem heater/sensor configuration allows for better comparison with experiments; figures 3-5 show the results [4]. Modeling PMOS devices necessitates the inclusion of hole transport and hole-phonon interactions. Finally, the analysis of CMOS logic circuits using this device simulation methodology uses parametric iteration. The device model treats contacts as Direclet boundaries, iteratively applying a fixed potential at each contact node then checking for current continuity. In simulating a CMOS inverter, the extracted voltage transfer curve shown in figure 6 demonstrates the procedure and efficacy of this methodology. This work demonstrates the effectiveness of the dual-carrier electrical solver in simulating CMOS circuits. Future work requires the coupling the dual-carrier electrical solver with the proven thermal solver to provide electro-thermal simulations of CMOS systems.

[1] C. Jacoboni, The Monte Carlo Method for Semiconductor Device Simulation. Wein ; New York: Wein ; New York : Springer-Verlag, 1989.

[2] E. Pop, S. Sinha and K. E. Goodson, "Heat Generation and Transport in Nanometer-Scale Transistors," Proc IEEE, vol. 94, (8), pp. 1587-1601, 2006.

[3] K. Raleva et al, "Modeling Thermal Effects in Nanodevices," Electron Devices, IEEE Transactions on, vol. 55, (6), pp. 1306-1316, 2008.

[4] Daugherty, R., & Vasileska, D. (2017). Multi-Scale Modeling of Self Heating Effects on Power Consumption in Silicon CMOS Devices. IMAPS January 2017, Vol. 2017, No. DPC, pp. 1-22.

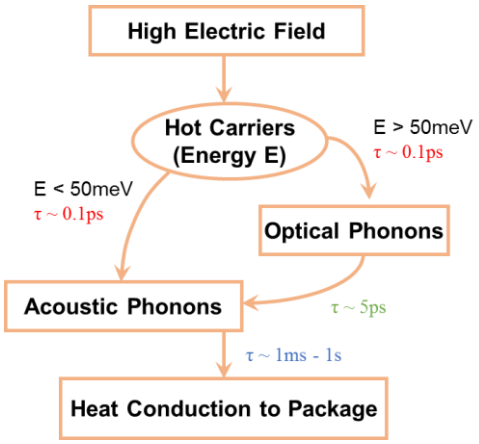

Fig.1: Overview of the thermal transport processes by which high energy carriers interact with phonons. Modeling the contribution of optical phonons requires device level simulation, while the wide variance in the time scales necessitates a multi-scale approach.

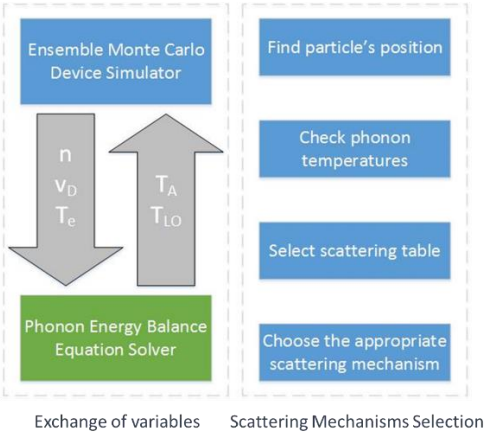

Fig.2: Coupling scheme to join the Monte Carlo/Poisson based electrical model with the energy balance carrier-phonon thermal transport model.

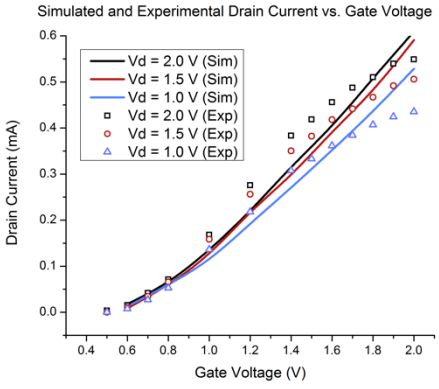

Fig.3: Comparison of experiment and simulation – IV characteristics of an NMOS active device paired with a common drain connected sub-threshold sensor.

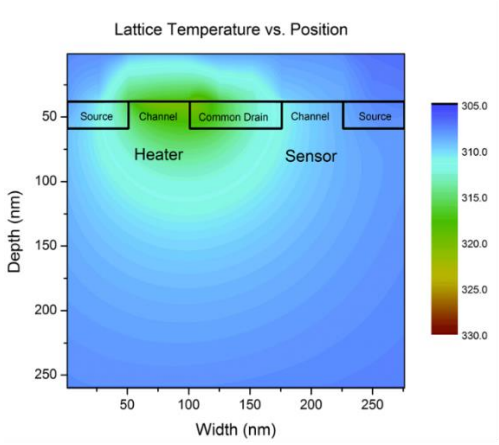

Fig.4 Comparison of experiment and simulation - simulated thermal profile of the lattice temperature in the active region of an NMOS device.

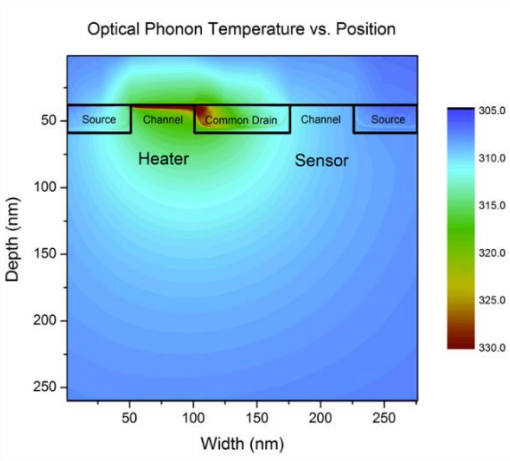

Fig.5 Comparison of experiment and simulation - simulated thermal profile of the optical phonons in the active region of an NMOS device.

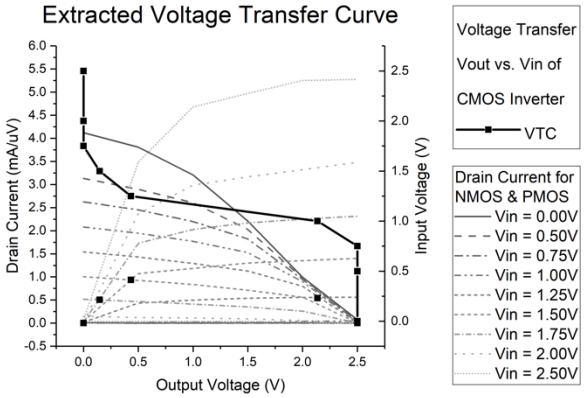

Fig.6: Voltage transfer curve of a simulated CMOS inverter. The output voltage is determined by treating contacts as Direchlet boundaries and looking for current continuity.