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P:25 Characterisation of a tunnel field-effect transistor using 2D TCAD simulations

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In conventional MOSFETs, the subthreshold swing (SS) has a fundamental limit of 60 mV/dec at room temperature that affects the minimum power consumption achievable when the device is turned off [1], [2]. Such constraint is one of the limiting factors of MOSFETs for low power devices. One of the promising solutions are tunnelling-FETs (TFETs) that demonstrated a much steeper SS with a very small leakage current (I_{OFF}) because their operation is based on the band- to-band tunnelling (BTBT). The main drawback of TFETs are their low on-current (I_{ON}) [3]–[5]. Various approaches aim to overcome the (I_{ON}) issue and one of them, examined in this paper, is a modified structure of a conventional TFET by adding an extra layer between the gate-dielectric and the *p-i-n* junction to increase the tunnelling area. The aim of this paper is to investigate the performance of a parallel electric field (PE) TFET based on the experimental device [4].

The device is an *n*-type PE-TFET with a gate length of 1 μm as shown in Fig. 1. The epi-layer and the SOI have an intrinsic doping of 1.0×10^{15} cm^{-3}, the *p*-type source has a concentration 3.7×10^{19} cm^{-3} and the *n*-type a doping of 2.7×10^{20} cm^{-3}. The work function of the metal gate (TiN) is 4.8 eV. Simulations have been performed using Silvaco ATLAS version 5.20.2.R [6]. The simulations account for both the local and non-local BTBT, for the band-gap narrowing (BGN), the local and non-local trap assisted tunnelling, the Shockley-Read-Hall recombination, Auger generation, the impact ionization effects and finally the thermionic emission transport model at semiconductor-semiconductor interfaces.

Fig. 2 shows the I_D–V_G characteristics at high (1.0 V) drain bias comparing simulations with experimental data which is very close at large gate biases. The simulations can reveal details of device architecture since IOFF increases dramatically with a drain-to-gate distance (D) while (I_{ON}) shows a minimal change. They determine $D \leq$ 5 nm as oppose to experimentally reported of 20 nm which would underestimate I_{OFF} by orders of magnitude. Fig. 3 shows that electron density is larger near the epi-channel junction when the $D =$ 0 nm than $D =$ 5 nm which results in a larger I_{OFF}. Fig. 4 shows a band- profile when the device is in OFF- ($V_G =$ 0.3 V) and ON- mode ($V_G =$ 2.5 V), respectively, for $D =$ 0 and $D =$ 5 nm at $V_D =$ 1.0 V. Note that at the OFF-mode, the current is due to the tunnelling near the drain side while, at the ON-mode, the tunnelling current occurs both near the epi-layer edge on the source side as well as at the source-intrinsic layer junction. The change in D from 0 to 5 nm reduces the I_{OFF} around 90% and introduces a shift of 0.1 V in the V_G. Fig. 5 shows that as the relative permittivity (*Er*) of the high-κ layer under the gate is increased, the $I_D - V_G$ curve shifts upwards (increased current). Fig. 6 shows how the doping of the source and drain regions affects the performance of the device. A decrease in the source doping by 35% will decrease the ON-current by around 48% at VG = 2.5 V and $V_D =$ 1.0 V while an increased in the drain doping by 48% increases the OFF-current by about 58% at $V_G =$ 0.5 V and $V_D =$ 1.0 V. Fig. 7 studies the effect of the LOV length. When LOV is reduced from 150 nm to 100 nm, the current at $V_G =$ 2.5 V and $V_D =$ 1.0 V is reduced by around 23%. Finally, Fig. 8 shows variations in a thickness of the epi-layer from 2 nm to 1 and 3 nm and found that as the epi-layer thickness is increased the I_D is reduced for all the V_G.

We have simulated an *n*-type PE-TFET device with 1.0μm gate length using DD simulations enhanced by tunnelling models calibrated against the experimental device in Ref. [4] with a good agreement at low and high drain biases. The most significant outcome of this study is that the distance between the gate and drain
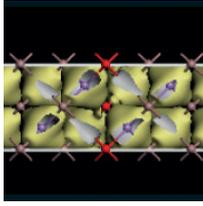
region significantly affects the I_{OFF} while no significant change occurs for the I_{ON}. We have also studied how the ϵ_r of the high-κ, doping of the source/drain region, the length of the L_{OV}, and the epi-layer thickness affect the PE- TFET characteristics. This work can serve as a good base for the guidance to design TFETs with optimal on-off ratios for future low-power applications, or to optimize other parameters to enable Internet-of-Things (IoT) devices.
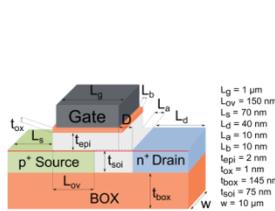
Fig. 1. Schematic of the PE-TFET with the corresponding dimensions. The z-direction is assumed to be 10 μm wide.
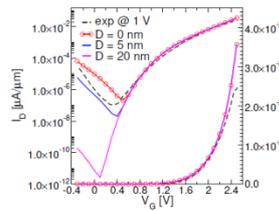
Fig. 2. $I_D - V_G$ characteristics on both linear (right) and logarithmic (left) scales at a high drain bias of 1.0 V when the distance (D) is varied.
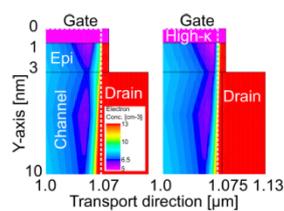
Fig. 3. Electron density on the drain side at $V_D = 1.0$ V and $V_G = 0.3$ V for $D = 0$ nm (left) and $D = 5$ nm (right). Dotted line indicates the end of the gate while the vertical black line indicates the junction at the channel-drain region.
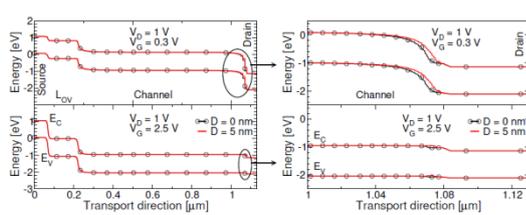
Fig. 4. The band profile (left) from the source to the drain close to the epi-layer (cut indicated by a red line in Fig. 1) as well as a close-up (right) of the channel-drain junction at $V_D = 1.0$ V, $V_G = 0.3$ V (OFF-mode) (top) and $V_G = 2.5$ V (ON-mode) (bottom). The black line with symbols corresponds to the device with $D = 0$ nm and the red line without symbols to the device with $D = 5$ nm.
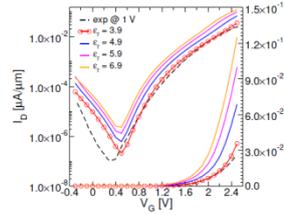
Fig. 5. I_D–V_G characteristics on both linear (right) and logarithmic (left) scales at a high drain bias of 1.0 V when the ϵ_r of the high-κ layer under the gate is varied.
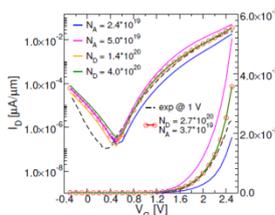
Fig. 6. I_D–V_G characteristics on both linear (right) and logarithmic (left) scales at a high drain bias of 1.0 V when the doping in the drain (N_D) or the source (N_A) region is varied.
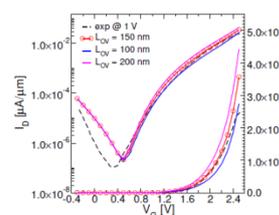
Fig. 7. I_D–V_G characteristics on both linear (right) and logarithmic (left) scales at a high drain bias of 1.0 V when the distance (L_{OV}) of the source region under the gate is varied.
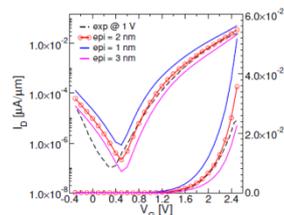
Fig. 8. I_D–V_G characteristics on both linear (right) and logarithmic (left) scales at a high drain bias of 1.0 V when the thickness of the epi-layer is varied.

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