P:24 Towards a full self-consistently coupled drift diffusion and Monte Carlo simulator to model silicon heterojunction solar cells

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The Drift-Diffusion (DD) model has been extensively used to model solar cells of all types. This model provides an efficient and reasonably accurate way to simulate solar cells as long as the physics doesn't stray too far away from the assumptions used to derive the DD model. However, with the advent of 2nd and 3rd generation solar cells [1], novel device structures and new materials have tested the limits of traditional methods.

Our work focuses on an amorphous silicon (a-Si)/crystalline silicon (c-Si) heterojunction solar cell (SHJ), also referred to as a HIT cell [2]. The strong band bending and high electric field at the heterointerface of this cell leads to a non-Maxwellian energy distribution of photogenerated carriers [3]; this, in turn, violates some of the assumptions made in the derivation of the DD model from the Boltzmann transport equation (BTE). The DD model is not ideal for studying regions where the electric field varies rapidly over a very short distance; the distribution function becomes non local in such scenarios and the local electric field based description of the DD model is no longer applicable.

The Monte Carlo (MC) solution to the BTE is an ideal tool to study the distribution function in high field scenarios but has some limitations when it is considered as a global simulator. It becomes quite inefficient in regions where the field is low, whereas DD models can perform very efficiently and accurately in these areas. Thus, by coupling both these solvers it is possible to combine their advantages to create a computationally efficient and accurate solver [4].

Coupled DD and MC hybrid solvers have been implemented in the past to study hot carrier effects in MOSFET's [5]. In this paper we have utilized this concept to study high field effects and interfacial transport in a SHJ solar cell. This is the first stage of our modeling effort to build a fully self consistent multiscale solver that can describe transport across various length and time scales.

The hybrid solver consists of a DD solver and an MC solver. The DD solution is applied to the quasi-neutral areas which have low electric fields and the MC solution to the regions near the heterointerface which have high electric fields.

At first the DD solution is applied to the entire SHJ to determine the fields, potentials, carrier densities and currents in the device. Then the region to apply the MC solution is identified based on a critical electric field. Special care has to be taken to make sure the input carrier distribution is strongly correlated to the DD solution at the MC-DD boundary [6].

The initial DD solution calculates the current that in turn serves as the flux boundary condition for the MC. Figure 1. shows a schematic diagram of the HIT cell and the different domains that are being implemented to realize the multiscale solver; in previous works we have developed the MC and kinetic Monte Carlo (KMC) modules [7]. The solvers are said to be current matched when the MC solver reproduces the DD injection current. The current is calculated by analyzing the slope of the cumulative charge vs. time.

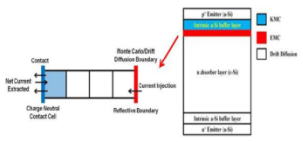

Fig 1. (Right) Schematic diagram of HIT cell and the different simulation domains. (Left) Schematic representation of the boundary conditions for MC - DD coupling.

The MC solver treats photogenerated holes at the heterointerface [8]. The MC solver is placed in the depletion region of a p-i-n junction on the 'n' side which gives rise to some crucial problems. There is orders of magnitude difference in hole density in terms of the densest cell and the least dense cell which leads to a lot of noise in the extracted current from the MC. We make some assumptions to account for the generation and recombination process that take place near a contact in a solar cell. The application of a MC solver is applicable if, 1) it is placed in an area where the photogenerated carriers have a diffusion length greater than its distance to the contact and 2) it is placed close to the front contact where the high frequency photo generation is not going to contribute to the short circuit current.

Once the solvers are current matched, coupling coefficients are extracted from the MC and the DD equations are solved again to get the new injection conditions for the MC [9]. Thus, the self consistent Gummel loop is completed.

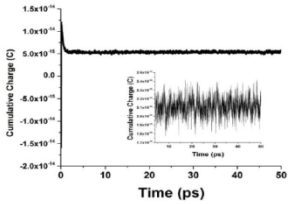

Fig 2. Cumulative charge vs. time extracted from the MC domain.

Figure 2 shows a cumulative charge vs. time plot for an injection of 50 mA/cm2 into the MC domain. The vastly varying carrier density in the domain combined with low current injection makes it very hard to extract a coherent slope by creating a lot of noise in the MC results.

The time taken for the simulations are heavily dependent on the current injection from the DD and the MC domain population describing the depletion region charge density.

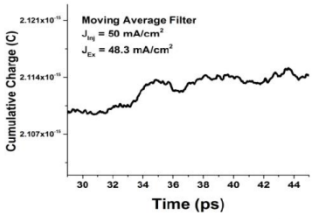

Fig 3. Moving average filter applied to fig. 2.

Figure 3 shows a moving average filter that is applied to the cumulative charge in order to reduce the noise. The solvers are said to be current matched if the injection current lies within ± 3σ of the extracted current. By following the method described in this paper we are able to current match the DD and the MC solvers. Our current work is focused on extracting coupling coefficients from the MC to complete the self consistent Gummel cycle.

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P:25 Characterisation of a tunnel field-effect transistor using 2D TCAD simulations

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In conventional MOSFETs, the subthreshold swing (SS) has a fundamental limit of 60 mV/dec at room temperature that affects the minimum power consumption achievable when the device is turned off [1], [2]. Such constraint is one of the limiting factors of MOSFETs for low power devices. One of the promising solutions are tunnelling-FETs (TFETs) that demonstrated a much steeper SS with a very small leakage current (I_{OFF}) because their operation is based on the band- to-band tunnelling (BTBT). The main drawback of TFETs are their low on-current (I_{ON}) [3]–[5]. Various approaches aim to overcome the (I_{ON}) issue and one of them, examined in this paper, is a modified structure of a conventional TFET by adding an extra layer between the gate-dielectric and the *p-i-n* junction to increase the tunnelling area. The aim of this paper is to investigate the performance of a parallel electric field (PE) TFET based on the experimental device [4].

The device is an *n*-type PE-TFET with a gate length of 1 μm as shown in Fig. 1. The epi-layer and the SOI have an intrinsic doping of 1.0 $\times$ 10^{15} cm^{-3}, the *p*-type source has a concentration 3.7 $\times$ 10^{19} cm^{-3} and the *n*-type a doping of 2.7 $\times$ 10^{20} cm^{-3}. The work function of the metal gate (TiN) is 4.8 eV. Simulations have been performed using Silvaco ATLAS version 5.20.2.R [6]. The simulations account for both the local and non-local BTBT, for the band-gap narrowing (BGN), the local and non-local trap assisted tunnelling, the Shockley-Read-Hall recombination, Auger generation, the impact ionization effects and finally the thermionic emission transport model at semiconductor-semiconductor interfaces.

Fig. 2 shows the I_D–V_G characteristics at high (1.0 V) drain bias comparing simulations with experimental data which is very close at large gate biases. The simulations can reveal details of device architecture since IOFF increases dramatically with a drain-to-gate distance (*D*) while (I_{ON}) shows a minimal change. They determine $D \leq 5$ nm as oppose to experimentally reported of 20 nm which would underestimate I_{OFF} by orders of magnitude. Fig. 3 shows that electron density is larger near the epi-channel junction when the *D* = 0 nm than *D* = 5 nm which results in a larger I_{OFF}. Fig. 4 shows a band- profile when the device is in OFF- (V_G = 0.3 V) and ON- mode (V_G = 2.5 V), respectively, for *D* = 0 and *D* = 5 nm at V_D = 1.0 V. Note that at the OFF-mode, the current is due to the tunnelling near the drain side while, at the ON-mode, the tunnelling current occurs both near the epi-layer edge on the source side as well as at the source-intrinsic layer junction. The change in *D* from 0 to 5 nm reduces the I_{OFF} around 90% and introduces a shift of 0.1 V in the V_G. Fig. 5 shows that as the relative permittivity (*Er*) of the high-κ layer under the gate is increased, the I_D – V_G curve shifts upwards (increased current). Fig. 6 shows how the doping of the source and drain regions affects the performance of the device. A decrease in the source doping by 35% will decrease the ON-current by around 48% at VG = 2.5 V and V_D = 1.0 V while an increased in the drain doping by 48% increases the OFF-current by about 58% at V_G= 0.5 V and V_D = 1.0 V. Fig. 7 studies the effect of the LOV length. When LOV is reduced from 150 nm to 100 nm, the current at V_G = 2.5 V and V_D = 1.0 V is reduced by around 23%. Finally, Fig. 8 shows variations in a thickness of the epi-layer from 2 nm to 1 and 3 nm and found that as the epi-layer thickness is increased the I_D is reduced for all the V_G.

We have simulated an *n*-type PE-TFET device with 1.0μm gate length using DD simulations enhanced by tunnelling models calibrated against the experimental device in Ref. [4] with a good agreement at low and high drain biases. The most significant outcome of this study is that the distance between the gate and drain