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P:23 Impact of the gate and external insulator thickness on the static characteristics of ultra-scaled silicon nanowire FETs

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The geometries routinely considered for the numerical simulation of nanoelectronic devices within quantum self-consistent models do not result in a realistic description of the electrostatic potential in the insulator covering the access regions. The thickness chosen for this latter is indeed tipically too small with respect to the decay length of electric field and the gate is modeled with thickless stripes, preventing any account for fringe fields. More realistic geometries are considered only in the framework of simpler transport models, in order to provide semianalytical descriptions of parasitics [1], [2], [3] or perform extensive explorations of the design parameter space [4], [5].

We propose a full quantum simulation study focusing on gate-all-around ultra-scaled silicon nanowire field effect transistors (NW FETs), aimed to investigate the impact of extending the simulation domain so as to include a larger part of the gate electrode and of the insulator enveloping the source and drain extensions.

Our simulation approach relies on an effective mass Hamiltonian fitted on tight-binding band structure computations [6] and is based on the self-consistent solution of the transport equations within the non-equilibrium Green's function formalism and of the Poisson equation. The electron scattering with acoustic and optical phonons is taken into account within the self-consistent Born approximation.

The geometries compared in this study are sketched in Fig. 1. The geometry A is the simplest and most widely used one, in which the gate corresponds to a wrapping surface belonging to the boundary of the simulation domain. On the contrary, the geometry B models the gate as a three-dimensional shell; the value of 5 nm set for its thickness has been verified to guarantee a reasonable stabilization of the results against any further increase. In order to investigate the interplay with different degrees of quantum confinement and short channel effects, we consider NW FETs with two different transversal crosssections (2x2 and 5x5 nm^2), gate lengths (5 and 10 nm) and gate underlaps (0 and 3 nm).

Our results highlight deviations between the two models both in the subthreshold region and at large gate overdrives. As illustrated in Fig. 2 and in the top panel of Fig. 3, accounting for the fringe field of the gate in the B arrangement can dramatically improve the electrostatic integrity and consequently the subthreshold swing with respect to the A case. This effect is particularly pronounced in the wider and shorter devices, as a consequence of the less effective gate control. In the narrower devices, due to the weaker pinning in the doped source region, at large overdrive the gate fringes can induce a sizeable bottom shift in the lowest subband with respect to the A case (bottom panel of Fig. 3). This effect, stronger in the ballistic regime and quite weakly dependent on the gate length, results in an increase of the current in the B arrangement with respect to the A one. The overall impact on the estimation of the device performance for several representative configurations is summarized in Table1, which indicates that the I_{ON}=I_{OFF} ratio computed with the A geometry can suffer from large underestimations as compared to the results obtained with the B geometry.

The discrepancies between the two models in terms of sensitivity to the discrete dopant variability are addressed in Fig. 4 and Fig. 5. Two arrangements of discrete dopants, denoted as (1) and (2), are considered, differing in the distance between the dopants and the gated region of the nanowires. The difference of the currents in the case (1) and (2) divided by their average is taken as a measure of the sensitivity of the devices. A close inspection of the curves in Fig. 5 for high values of the gate voltage indicates that the relative deviation of the sensitivity between the devices described with the model A or B can be significant.

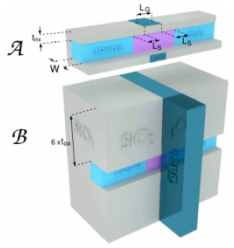

Fig. 1. Sketch of the considered geometries. SiO_2 is chosen as the insulator material. The gate oxide thickness is $t_{ox} = 1$ nm. The source and drain extensions are 12 nm long and are n-doped with concentration 10^{20} cm^{-3}. L_G and L_S denote the gate and spacer length, respectively.

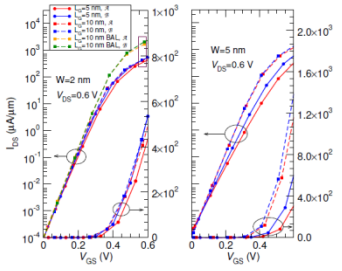

Fig. 2. Transfer characteristics for nanowires with $W = 2$, 5 nm, $L_G = 5$, 10 nm and $L_S = 3$ nm. For the case $W = 2$ nm and $L_G = 10$ nm also the ballistic curves (BAL) are shown. All the curves have been horizontally shifted in order to set $I_{DS} = I_{OFF} = 10^{-4}$ μA/μm at $V_{GS} = 0$ V.

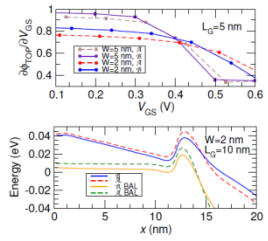

Fig. 3. *Top*: derivative of the potential ϕ_{TOP} of the top of the source-to-drain barrier with respect to the gate voltage corresponding to some of the transfer characteristics in Fig. 2. *Bottom*: detail of the lowest subband in the source region corresponding to the points enclosed within a rectangle in Fig. 2. The subbands referring to the dissipative regime have been vertically shifted of 0.02 eV for clarity. The Fermi level at the source contact equals 0 eV.

	$L_S = 3$ nm				$L_S = 0$ nm	
	$L_G = 5$ nm		$L_G = 10$ nm		$L_G = 5$ nm	$L_G = 10$ nm
	BAL	PHON	BAL	PHON	PHON	PHON
$W = 2$ nm	53%	28%	26%	10%	26%	6%
$W = 5$ nm	122%	117%	21%	20%	516%	13%

TABLE I

PERCENTAGE INCREASE OF THE I_{ON}/I_{OFF} RATIO IN THE $\mathcal{B}$ GEOMETRY WITH RESPECT TO THE $\mathcal{A}$ ONE IN THE BALLISTIC (BAL) AND DISSIPATIVE (PHON) REGIME. I_{OFF} IS SET TO 10^{-4} μA/μm.

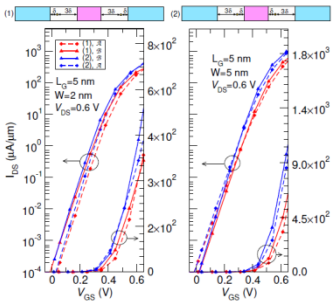

Fig. 4. Transfer characteristics for nanowires with $W = 2$, 5 nm and $L_G = 5$ nm in the presence of two discrete dopants at the center of the nanowire transversal cross-section, located symmetrically with respect to the gate. The top of the figure illustrates the two different arrangements considered, denoted by (1) and (2). δ =1.5 nm. Each couple of curves $\{I_{DS}^{(1)}, I_{DS}^{(2)}\}$ referring to the same geometry has been horizontally shifted in order to set to 10^{-4} μA/μm the value of the arithmetical average $(I_{DS}^{(1)} + I_{DS}^{(2)})/2$ at $V_{GS} = 0$ V.

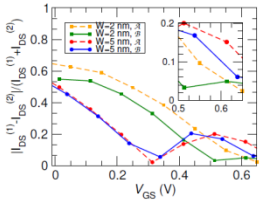

Fig. 5. Deviation of the value of the current relative to the average $|I_{DS}^{(1)} - I_{DS}^{(2)}|/(I_{DS}^{(1)} + I_{DS}^{(2)})$ for the couples of transfer characteristics $\{I_{DS}^{(1)}, I_{DS}^{(2)}\}$ in Fig. 4 referring to the same geometry and to a different arrangement of dopants. The inset shows an enlargement for high V_{GS}.

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