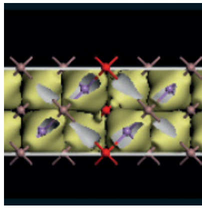

P:16 Scaling of Tunnel FETs

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Scaling of tunnel FETs is discussed using device simulation with nonlocal band-to-band tunneling model. Impacts of channel length, drain dopant level, SOI (or Fin) thickness are systematically investigated. The effects of the scaling are quite different from those of conventional MOSFETs, especially for their channel thickness dependence.

Tunnel FET (TFET) is a potential candidate for the low power transistor as an alternative to a MOSFET [1]. The authors developed several types of TFETs on matured silicon technology. These TFETs are successfully modeled by device simulation with the nonlocal band-to-band tunneling (BTBT) model [2][3], and recently, the drain bias dependence of long channel TFET characteristics is well explained by the same approach [4]. These series of studies are the base for further investigations of the scaling of TFETs, which is an important issue to determine the future of TFETs.

Fig. 1 shows the cross sections of p-type silicon (a) SOI and (b) Fin TFETs discussed in this work. For simplicity, source and drain junctions are at the gate edges, channel dopant is constant and weakly p-type, effective oxide thickness is 1 nm, the supply voltage is 0.5 volt. The nonlocal BTBT model is implemented as in ref. [1]. The drain bias dependence of an SOI TFET with a gate length of 500 nm is shown in Fig. 2, and the physics behind the dependence is discussed in ref. [4].

Gate length dependence of the SOI TFET I_D-V_G characteristics is shown in Fig. 3. Below 10 nm, the source-to-drain direct tunneling is caused which cannot be controlled by gate voltage. This punch-through between source and drain may be weakened by low drain dopant concentration, such as 1018 cm-3, but not so effectively.

Fin-TFET realizes the double current compared with the SOI-TFET both for on- current (I_{ON}) and off-current (I_{OFF}) as shown in Fig. 4 (a). Fin-thickness dependence is also shown in Fig. 4 (a), where (I_{OFF}) increases more than I_{ON} for thinner fins. In Fig. 4 (b), the same curves are adjusted to the same IOFF's by changing the gate work-functions. The I_{ON} increases for the same I_{OFF} for fin thicknesses below 10 nm.

Fig. 5 shows fin thickness dependence of gate length 10 nm TFETs. The fin thickness scaling is not so effective in suppressing the short channel punch-through.

Fig. 6 shows two-dimensional distribution of the BTBT generation rates for the gate length of 30 nm and the fin thickness of 5 nm. Hole generation rate peaks for the front and the back gates are located nearly at the center of the fin thickness, and the electric field becomes larger under the control of the front and back gates.

Effects of TFET device scaling are studied using device simulation. Channel length affects I_{ON} - I_{OFF} below 20 nm, and source-to- drain punch-through occurs below 10 nm. In Fin-type TFETs, I_{OFF} increases for thinner Fin above 20 nm more than I_{ON}. When I_{OFF} is adjusted, I_{ON} increases for fin thickness below 7 nm. However the fin thickness scaling is not effective for short channel punch-through of gate length below 10 nm. Thus TFET-scaling is quite different from MOSFET-scaling.

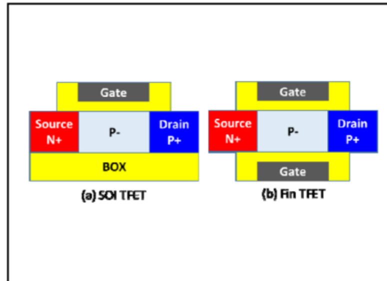

Fig. 1. Schematics of (a) SOI and (b) Fin TFETs studied in this work.

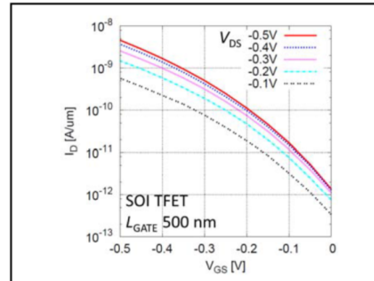

Fig. 2. Drain bias dependence of I_D-V_G characteristics of an SOI TFET of a 500 nm gate length.

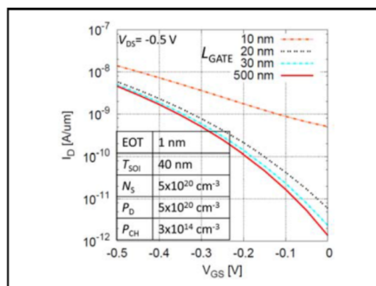

Fig. 3. Channel length dependence of I_D-V_G characteristics of the SOI-TFET.

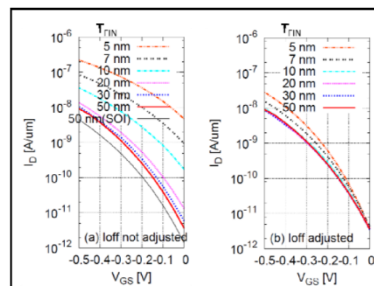

Fig. 4. Thickness dependence of Fin TFET characteristics (a) without and (b) with I_{OFF} adjustment. L_{GATE} is 500 nm.

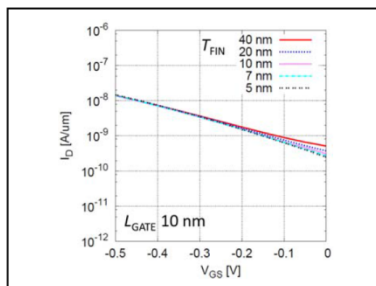

Fig. 5. Fin thickness dependence of Fin TFET with gate length of 10 nm. Short channel punch-through is not suppressed effectively by fin-thickness scaling

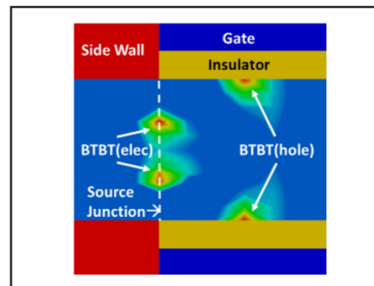

Fig. 6. 2D distribution of the BTBT generation rates for L_{GATE}=30 nm and T_{FIN}=5 nm case. The gate and drain voltages are -0.5 V.

[1] Ionescu, A. M., and H. Riel, Nature 479.7373, 2011.

[2] K. Fukuda et al. "On the nonlocal modeling of tunnel-FETs." SISPAD, 2012.

[3] K. Fukuda et al. "Predictivity of the non-local BTBTmodel for structure dependencies of tunnel FETs." IWCE, 2014.

[4] K.Fukuda et al., "On the drain bias dependence of tunnel FETs," Proc. SSDM, 2016.