P:13 Multi-subband ensemble Monte Carlo simulator for 3D electron devices

L Donetti, C Sampedro, F G Ruiz, A Godoy and F Gamiz

Universidad de Granada, Spain

To study non-planar MOS devices with multiple gates we have developed a Multi- Subband Ensemble Monte Carlo (MS- EMC) simulator for 3D devices, coupling the solution of 3D Poisson Equation (PE), 2D Schrödinger Equation (SE) and 1D MC transport.

II. THE SIMULATOR

To simulate a 3D device we employ the space-mode approach [1], where the SE is solved in several cross sections of the device perpendicular to the transport direction. The MC approach is then applied to carriers in every subband considering 1D transport. Self-consistency is obtained by solving the 3D PE in the whole device.

A flow chart of the simulation strategy for a given value of the gate bias V_G is reported in Fig. 1. The algorithm starts with V_{DS}=0 V and a self-consistent solution of SE and PE in equilibrium (w/o transport) is found employing a predictor-corrector method. This allows the initialization of the MC simulator employing the equilibrium Fermi- Dirac distribution for each subband. Then a self-consistent MC, PE, SE loop is started. In a first phase the boundary conditions at the drain are changed step by step in order to reach the desired value of V_{DS}. After that, the boundary conditions are kept fixed while a self-consistent solution for the potential is reached within a prescribed tolerance. Finally, the current is computed while preserving self-consistency. This self- consistent procedure is repeated for increasing values of V_{DS}.

The simulation domain is represented using a 3D finite element mesh: first a 2D triangular mesh of the device cross section is built and then the 3D one is built by extrusion. The finite element mesh allows a good representation of complex geometries (e.g. round nanowires, rounded corners, leaning sidewalls in FinFETs) and a natural formulation of the equations (PE, SE) near material boundaries. Different properties are mapped to nodes (e.g. the potential), to elements (e.g. affinity, dielectric constant, energy gap, etc.) or even on nodes as seen from each element (for example the conduction band which depends on both the electrostatic potential of the node and the material properties of the element).

The SE is solved in several 2D cross sections of the device employing triangular finite elements. Non-parabolic corrections are added to energy levels and to the band structure [2]. To improve the MC statistics, especially in the sub-threshold regime, non-uniform particle weights are employed which depend on particle energy [3]. At this stage acoustic and optical phonon scattering has been implemented [4]. For the scattering events, the simulator takes into account the Pauli's exclusion principle: to do that the occupation function $f_{\mu i}(k)$ is computed and updated for every subband μ and cross-section i [5].

We simulated FET devices based on Si nanowires in ‹100› direction with diameter D=6 nm, SiO_2 thickness T_{ox}=1 nm, gate length L_G=14 nm, undoped channel and gate work function 4.65 eV. Source and drain doping is N_{SD}=1×10^{20} cm^{-3}, with underlap L_{sp}=2 nm and Gaussian distribution with σ=0.8 nm. Some results are shown in Figs. 2-8, including electron wave- functions, output and transfer characteristics, subband energy profiles and populations. In Fig.4 we compare the subthreshold behavior of devices with L_G down to 8 nm: notice that the statistical error is relevant only for current values < 1 nA.

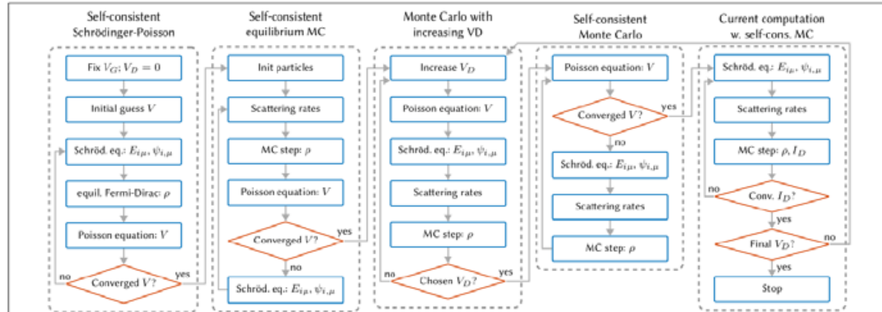

Fig. 1: Block diagram for the simulation of an I_D-V_D curve, which is repeated, if needed, for different values of V_G.

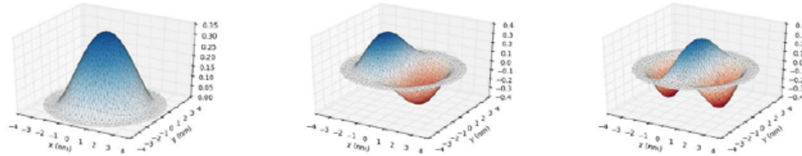

Fig. 2:Wave functions of the first 3 subbands of the Δ_1 valley in the middle of the channel for V_G=0.5 V, V_D=0.05 V.

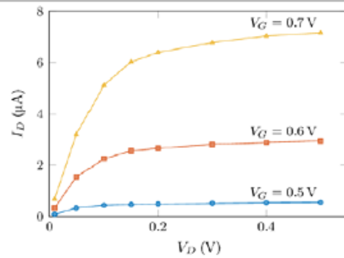

Fig. 3: Output characteristic of the device with L_G=14 nm.

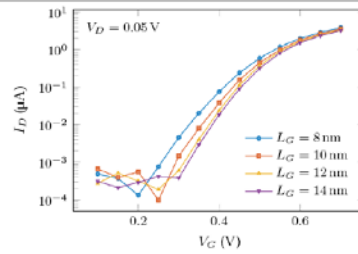

Fig. 4: Transfer characteristic of devices with different L_G.

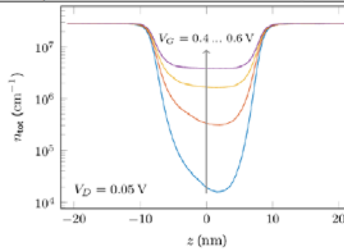

Fig. 5:1D electron density for different values of V_G.

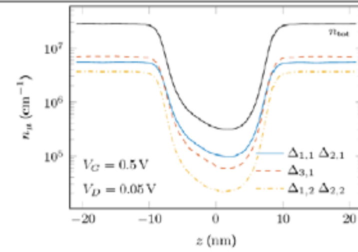

Fig. 6: Population of the lowest energy subbandds.

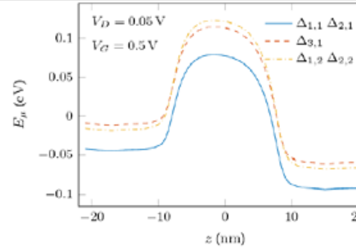

Fig. 7: Energy profile of the lowest energy subbands.

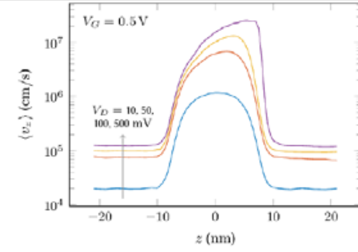

Fig. 8: Average velocity profiles for increasing values of V_D.

[1] R. Venugopal, Z. Ren, S. Datta, M. S. Lundstrom, and D. Jovanovic, Journal of Applied Physics, 92(7), p. 3730, 2002.

[2] S. Jin, M. V. Fischetti, and T.-w. Tang, Journal of Applied Physics 102, p. 083715, 2007

[3] A Pacelli1, U Ravaioli, Solid-State Electronics, 41(4), p. 599, 1997.

[4] A. Godoy, F. Ruiz, C. Sampedro, F. Gámiz, U. Ravaioli, Solid-State Electronics 51, p. 1211, 2007.

[5] P. Lugli and D.K. Ferry, IEEE Transactions on Electron Devices 32(11), p. 2431, 1985.