P:03 The impact of interface traps and self-heating in the degradation of the 4H-SiC VDMOSFET performance

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Silicon carbide (SiC) material is an ideal candidate to replace silicon (Si) for high temperature, high power device applications. This is due to its excellent physical and electronic properties such as a large band gap, high critical electric field, high thermal conductivity and high saturation velocity. SiC devices are ideal as high power switches and rectifiers for both low and high frequency applications [1]. Although there has been substantial improvements in the material technology, the quality of the oxide interface represents an issue for the reliability of these devices. The presence of unwanted traps at the interface degrades the device performance.

In this work, we study the impact of interface traps in the device performance. We also explore the interplay between traps and the self-heating effects.

The effect of self-heating is studied by comparing with the measured *I-V* curves of a commercial device, C2M1000170D 1.7KV 4H-SiC vertical DMOSFET half-cell for study [2].

We have done electrical characterisation and subsequently extracted the device doping, dimension and physical parameters. The donor concentration of P-epi region is N_D = 3×10^{15} cm^{-3}. The gate oxide thickness was set to around 90nm and the channel length is 3.5µm. The layout and dimension of the device half cell is shown in Fig. 1.

Device simulations were carried out using a commercial TCAD software package Atlas by Silvaco [3]. Drift-diffusion transport model were used in all simulations. Physics-based models were included to account for carrier mobility, carrier generation and recombination, impact ionization and lattice heating. The electrothermal simulations allows us to localize the hot spot for self-heating. Electro-thermal simulations including interface traps with a density of 10^{12} cm^{-2} were performed. The simulated current-voltage characteristics are in good agreement with the experimental one in a wide range of bias as shown in Fig. 2. In addition, the simulated characteristics which includes a model for self-heating produces a better agreement with the experimental results. In Fig. 3, we see a shift in the threshold voltage by about 2V when the effect of interface traps are taken into account while self-heating leads to a decline in the transfer characteristic for the case with and without interface traps. We observe an increase in the on-resistance when the interface traps and self-heating effect are incorporated (see Fig. 4). Note that the combined effects of interface traps and self-heating is not linear, i.e the decrease in the current is not a simple addition of the two mechanisms and this can be seen in Fig. 4. Notice the collapse of the drain current by 12.9% for self-heating only, 17.6% for interface traps only and 51.4% when the combined effects of self-heating and interface traps are considered. By comparing Figs. 5 and 6, the observed increase in the local temperature is reduced by the presence of interface traps as the current is small when the interface traps are considered. The region with very high temperature is correlated to the region where high electric fields are experienced. In conclusion, we have carried out electrothermal simulations of n-type 4H-SiC VDMOSFET. We have shown that self-heating substantially reduces the on-current whereas the presence of interface traps leads to a reduction in the maximum lattice temperature, the on-current and a shift in the threshold voltage.

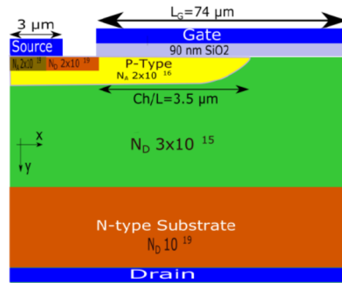

Figure 1: Structure of the SiC VDMOSFET

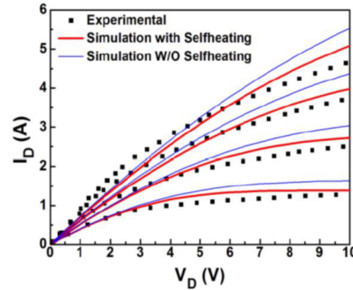

Figure 2: I_D-V_D Characteristics with and without self-heating

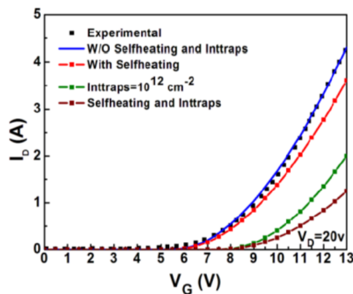

Figure 3: I_D-V_G characteristics with and without Interface traps and self-heating

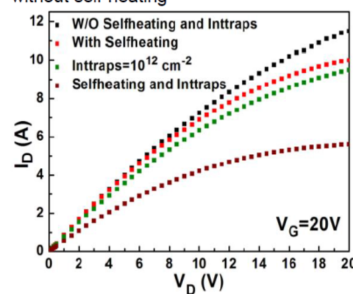

Figure 4: I_D-V_D at V_G=20V with and without interface traps and self-heating

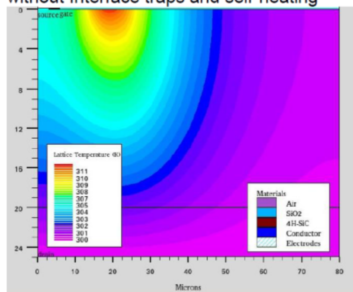

Figure 5: Lattice temperature assuming only self-heating in the device at V_G=20V

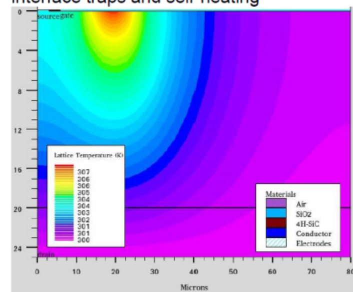

Figure 6: Lattice Temperature assuming both self-heating and Interface traps at V_G=20V

[1] M. Bhatnagar and B.J. Baliga, IEEE Trans. Electron Devices 40, 645 ,1993.

[2] CREE model C2M1000170D [online available: http://www.cree.com/~/media/Files/Cree/Power/Data%20Sheets/C2M1000170D.PDF]

[3] Silvaco, Atlas User ' s Manual, Santa Clara, CA:Silvaco Inc., 2016.