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DFT/NEGF study of discrete dopants in Si/GaAs 3D FETs including phonon scattering and self-heating

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Si FinFET nanowire transistors have been in production since 2010 and exhibit the promise of superior electrostatic and better performance than the planar MOSFET counterpart. As the size of the active regions of devices continues to be scaled down to nanometre dimensions, the number and location of a few impurities dramatically affect device performance. Tunnelling and confinement combined by strong local electrostatic potential invalidate the use of semi- classical models such as the drift-diffusion and Monte Carlo methods. The lack of validity of these methodologies to sub 10 nanometre dimensions is a direct consequence of the wave nature of the electron. Substantial work on discrete dopants has been carried out using a discrete point charge model in the NEGF formalism [1]. The density produced by this point model is mostly spherically symmetric or slightly deformed by the effective mass tensor. However, the wavefunction of the electron/hole occupying the dopant atom exhibits a tetrahedral symmetry and a shape dictated by the atomistic distribution of the surrounding. This can be seen in Fig. 1 and 2, which shows the absolute value of the wavefunction corresponding to an impurity embedded in Si and GaAs atom supercells. In the case of silicon, the dopant atom is Phosphorus and in the GaAs the dopant atom is Silicon. There is a concern of how reliable this point charge model is and what are the differences of using a more accurate description of the dopant and how much the I-V characteristic is changed by the use of this model. In this work, using non-equilibrium Greens Function (NEGF) formalism, we calculated the transfer characteristics of Si and GaAs nanowire transistors with a dopant in the middle of the channel [2]. The device has a 2.2 mm2 cross-section and a 6 nm channel length. The self- consistent electrostatic energy is shown in Fig. 4. We model the dopant atoms as a point charge, see Fig. 4, and also as a charge which reflects the DFT electron density. Scattering and self-heating are included. The calculation of the DFT dopant wavefunction is carried out with the Siesta code [3], using a supercell of 512 atoms. The ID-VG characteristics for the Si and GaAs devices are shown in Fig. 3, all simulations are done at VD = 0.4 V. In general, the current difference between the two dopant models is small. However, the difference is large in the case of GaAs. This difference can be attributed to the slight decrease in the source drain barrier height induced by the point charge. This effect can be observed by comparing the subbands in Fig. 5 and Fig. 6. These figures show the current spectrum and the first subbands for the 3 lowest Valleys of GaAs. Fig. 7 and 8 show the current spectra for the Si Device with DFT distributed charge at low and high drain. At low gate, the electron system heats up in the source and cools down at the drain, however at high gate bias the electron system is more efficient to dissipate the energy as the cooling of the electron system starts at the source- channel interface. It should be noted that for these devices there is a substantial amount of source to drain tunnelling. This can be observed in all the figures showing the current spectrum.

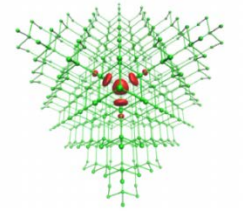

Fig. 1 Electron density of the LUMO in the 511 Si atoms supercell. The LUMO is centered in the P atom

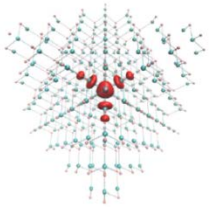

Fig. 2 Electron density of the LUMO in the 511 GaAs atoms supercell. The LUMO is centered in the Si atom

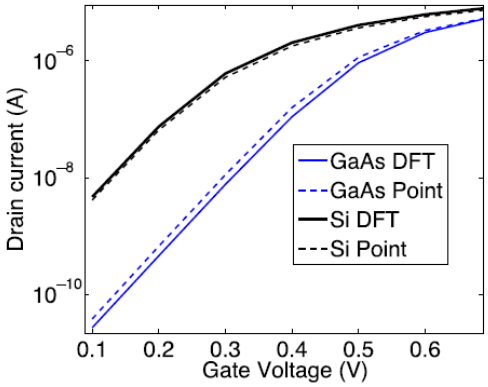

Fig. 3 I_D-V_G characteristic of Si and GaAs GAA nanowires with point/DFT charge density

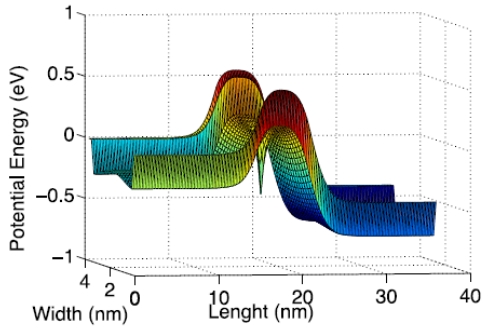

Fig. 4 Potential Energy along the channel and the one of the width for the point charge impurity.

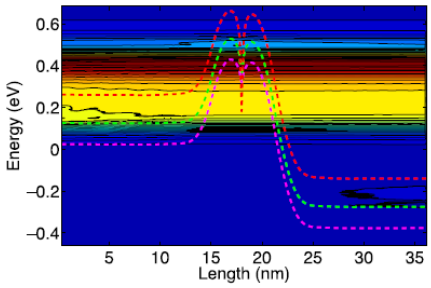

Fig. 5 Current spectrum for the GaAs device with a point charge. The subbands corresponding to the 3 lowest energy valleys are also shown. The point charge lower the energy barrier at the middle of the channel, V_g = 0.1 V

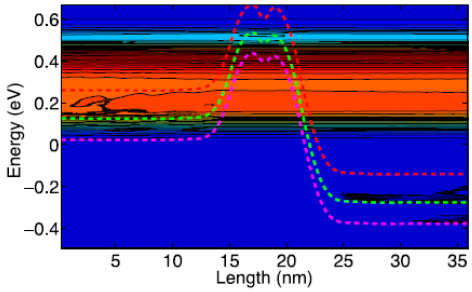

Fig. 6 Current spectrum for the GaAs device with a DFT distributed charge. The subbands of the three lowest valleys of GaAs are also shown, V_g = 0.1 V

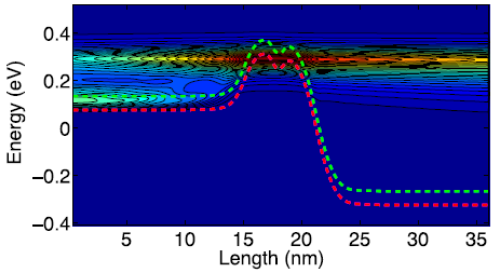

Fig. 7 Current spectrum for the Si device with a DFT distributed charge at V_g = 0.1 V

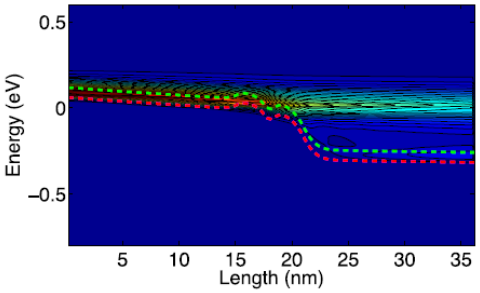

Fig. 8 Current spectrum for the Si device with DFT distributed charge at V_g = 0.7V

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Numerical techniques for the reduction of thermal conductivity measurements at nanoscale

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Nanostructuring offers the opportunity to increase the figure of merit of materials for thermoelectric applications, through the reduction of their thermal conductivity. The development of innovative anostructured materials for thermoelectric applications requires the improvement of techniques and rocedures for the reliable measurement of the thermal conductivity on a nanometric scale. Techniques for the measurement of thermal conductivity require heaters and temperature sensors (thermoresistors or thermocouples) whose width cannot be very small with respect to that of the nanostructures to be characterized. Conventional data analysis assumes that they are negligible, and can thus lead to misleading results. We propose to analyse the experimental measurements by means of finite element (FEM) modelling, taking into account the thermal and electrical transport both in the heaters/sensors and in the material to be characterized.

We present a numerical method for the characterization of thermal conductivity at the nanoscale with the 3ω technique[1]. This method has been applied to the analysis of experimental data for a device based on silicon nanomembranes, whose SEM image is shown in Fig. 1: a metal strip is fabricated on the suspended silicon structure, and is biased with a sinusoidal current; the amplitude and phase of the third harmonic of the voltage drop is measured in a four-probe configuration, through a lock-in amplifier. The key challenge of the 3ω technique is to develop suitable models for relating this third harmonic amplitude with the thermal conductivity of the structures under test. Analytical models have been developed in the past[2], assuming that: 1) the room temperature value of the heater resistance can be used for calculating the dissipated power; 2) the width of the heater is negligible with respect to the size of the structure to be measured; 3) the nanostructures are good electrical insulators. All these assumptions can lead to misleading results at the nanoscale. Our numerical technique consists in detecting the exact size both of the nanostructures and of the metal strip (heater) from SEM images; the thickness of the Si structures and of the metal heater is estimated from AFM images. This information is used to define a 3D model of the whole device (nanostructures and heater), for which we generate a discretization grid (see Fig. 2). Then, the electrical and thermal transport is simulated (within this 3D model) by means of the finite-element (FEM) technique, considering the thermal conductivity as a fitting parameter (see Fig. 3). An excellent fitting of the data can be obtained, overcoming the limits of conventional modelling (see Fig. 4). An automated procedure (Python code) for SEM photo survey, grid generation, and FEM simulation has been developed to achieve an acceptable throughput in the processing of experimental data.

We applied this method also to material deposited on top of suspended Si_3N_4 membranes (see Fig. 5). A metal heater has been considered in the middle of the nanomembrane, and the thermoelectric transport equations have been numerically solved for the thermal characterization of the material. Comparison with analytical models[1] will be reported.