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Simulation of negative differential transconductance from devices fabricated using conventional CMOS technology

P B Vyas[1], C Naquin[2], M Lee[2], W. G. Vandenberghe[1] and M V Fischetti[1]

[1]The University of Texas at Dallas, USA, [2]Texas Instruments Inc., USA

Negative differential transconductance (NDT) has been recently observed in Si CMOS devices using lateral quantum wells defined by ion implantation[1]. Here, we present a theoretical study[2] of these unique type of devices, emphasizing the limitations of their practical realization as well of our understanding of the basic physical processes involved. At the same time, we also indicate possible future promising paths that can help to achieve and optimize the observed quantum behavior at room temperature.

The aforementioned CMOS (nMOS) de- vices have a lateral quantum well (QW) built into the surface channel, formed by reversing the dopant polarity of the shallow source/drain (S/D) extensions (pSDE) from the standard n-type (for an nMOS transistor) to p-type, as sketched in Fig. 1. A two- dimensional (2-D) QW is formed when the gate-to-source voltage V_{GS} is large enough to invert the channel. Electrons injected into the channel at energies equal to the bound states, created by the 2-D confinement, un- dergo resonant or sequential tunneling. At certain gate biases, when the energy of the bound states will coincide with the Fermi energy of the electrons in the source, the source-to-drain current, I_{DS}, should exhibit sharp peaks. This observation of NDT in the $I_{DS} - V_{GS}$ characteristics is the motivation behind our investigation.

The simulation of the device characteristics[2] is done in 2 steps. First, we solve the 2-D single electron 'effective mass' Luttinger-Kohn (Schrödinger) equation under *closed* boundary condition self-consistently with the Poisson equation[3] with a source- to-drain bias V_{DS} = 0 and for several values of V_{GS}. As a second step, ballistic electron transport via tunneling through the confined states is studied by solving the Schro¨ dinger equation with *open* boundary conditions (Quantum Transmitting Boundary Method)[4] using the self-consistent potential distribution obtained from the previous step. This allows us to calculate the current-voltage characteristics.

Figs. 2 and 3 show that the lateral QW nMOS devices exhibit the desired NDT at low temperatures (∼10 K) and for gate lengths of the order of 20 nm and smaller. The strong dependence of I_{DS} on temperature indicate a significant presence of thermionic emission over the pSDE barriers. Punch-through cur- rent is also observed in these devices. The energy spacing between the quasi bound states (Fig. 4) suggest that devices with a gate length of 10 nm and lower should ex- hibit a sharp NDT signature even at room temperature, provided an optimal design can be found that minimizes thermionic emission (requiring high pSDE barriers) and punch- through (that meets the opposite requirement of potential-barriers low enough to favor the tunneling current). The former plays a crucial role in suppressing the NDT, the latter is favored over the tunneling current for high pSDE barriers. We are currently looking into silicon-on-insulator (SOI) devices with high pSDE barriers that can meet the requirements to exhibit NDT at room temperature.

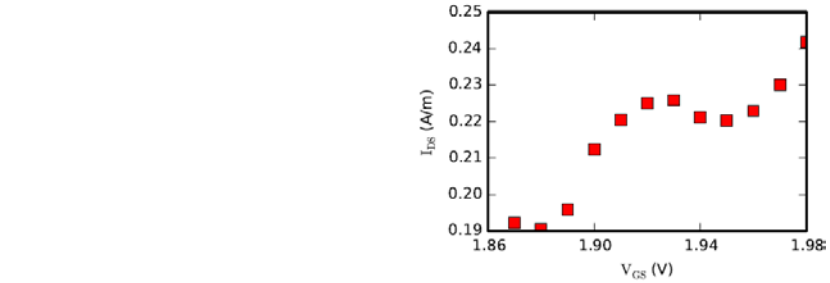

Fig. 3. Calculated $I_{DS} - V_{GS}$ characteristics for the 20 nm device at 10 K. V_{DS} = 1 mV.

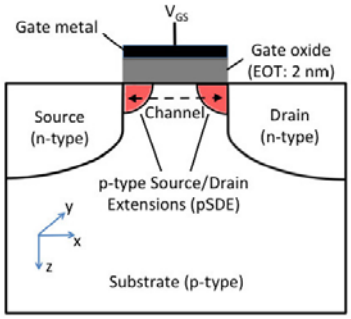

Fig. 1. Schematic cross-section of the lateral QW nMOSFET.

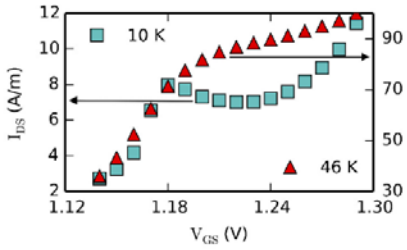

Fig. 2. Calculated $I_{DS} - V_{GS}$ characteristics at 46 K (black triangles) and 10 K (cyan circles) for the 10 nm device with V_{DS} = 10 mV.

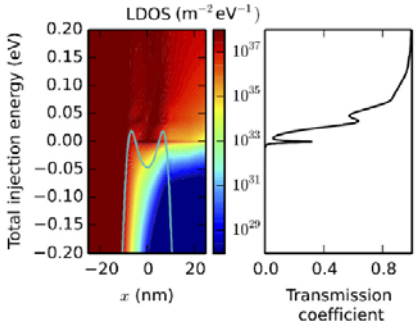

Fig. 4. Left: Average local density-of-states (LDOS) in the channel of the 10 nm device at 10 K. The cyan colored lines represent the potential-energy profile at the semiconductor/gate-insulator interface in each device. The energies are measured with respect to the Fermi energy in the source contact. Right: Transmission coefficient *vs.* injection energy for a particular traveling mode with energy -0.83 eV in the 10 nm device. V_{GS} = 1.18 V. The peaks in the transmission coefficient and the dark colored regions in the LDOS correspond to the quasi bound states in the channel.

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