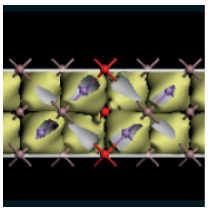

Variability-aware simulations of 5 nm vertically stacked lateral Si nanowires transistors

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In this work, we present a simulation study of vertically stacked lateral nanowires transistors (NWTs) considering various sources of statistical variability. Our simulation approach is based on various simulations techniques in order to capture the complexity in such ultra- scaled device.

Gate all around nanowire transistors (GAA NWTs) promise an improved transistor's electrostatics, offering better performance at lower supply voltages and significantly reducing the short channel effects. Arranging multiple GAA NWTs in vertically stacked lateral (VSL) configuration is a promising structure to increase the drive current for 7nm CMOS technology and beyond [1]. Also in current technology nodes, the variability is becoming important in nanoscale transistors due to process deviation and intrinsic properties of materials and interfaces. There are numerous sources of statistical variability (SV) such as Random Discrete Dopants (RDD), Wire Edge Roughness (WER) and Metal Gate Granularity (MGG), which dominate the NWT behaviour. Due to the inherited SV related to doping and gate patterning, it is very important to include SV information in process design kits (PDKs). Accurate statistical reliability (SR) information is crucial in defining the reliability criteria, and for supporting reliability-aware statistical design. For example, NBTI and PBTI degradations are associated with injection and trapping of carriers in defect states in the gate stack during device operation [2].

In this work, we study the SV of Si n-channel GAA NWTs with an elliptical cross-section of 7 nm x 5 nm. The device has a 0.4nm interfacial SiO_2 and 0.8nm HfO_2 (High-k) layers as shown in Fig.1. The doping concentrations are as follows: channel - $1014/cm^3$, source/drain extensions - $1020/cm^3$, and source/drain contacts - $4x1020/cm^3$. In our recently published work [3] we investigated the performance of vertically stacked lateral (VSL) NWTs. In this work, we examined the effects of SV and SR on the performance of VSL configured NWT. For this work two computational methods have been used: a Poisson-Schrödinger model (PS) coupled with Monte Carlo (MC) technique and quantum corrected drift-diffusion model. The flowchart in Fig. 2, illustrates the overall simulation methodology. The quantum corrections obtained from the Poisson-Schrödinger solution is used in the MC simulations to deliver predictive simulation results. Then the drift-diffusion simulator is calibrated against the MC result and used for efficient SV and SR simulations. An ensemble of 1000 devices has been simulated for the statistical analysis.

The simulated statistical ID-VG characteristics are shown in Fig 3(top). The correlation between different FOM as a function of trap density is shown in Fig. 4. The simulation data presented in Fig.5 include the main sources of SV and the interplay between interface traps and the FOM correlation. For example, the anti-correlation coefficient is lower (-0.95) between Ion and VT compared to when SV is not considered (-1) for VSL NWT with the double channels. Moreover, the distribution of ION and Ioff also shows more variability when both interface traps and sources of SV are considered as shown in Fig 5. Fig. 6 (top left) shows DIBL distribution for 1000 devices at five different scenarios. The average of the distribution is almost the same for all devices that include sources of SV (blue, red and black curves). The standard deviation is also very similar for those three cases and does not follow entirely the Gaussian distribution the two cases. When we consider only interface traps in the uniformly doped device, the DIBL has a lower value than in the other three scenarios where variability sources are included. Also for all cases the average value increases with increasing trap density in the oxide. Similarly, the distribution does not follow an entirely Gaussian distribution. Fig. 6 (bottom) present the Ion and IOFF current distribution for the ensemble of 1000 devices with and without sources of statistical variability and traps in the oxide, correspondingly. Like before the average value of both Ion and Ioff is shifted to higher values. Moreover, for all devices with included statistical variability, values of Ion and Ioff follow a Gaussian distribution. For the devices with interface traps

only and no variability sources the distribution is very similar in both cases. Fig. 6 (bottom right) reveals the threshold voltage distribution for all five scenarios. As expected when only the devices with statistical variability are considered, the average value of the distribution increases because of increasing the charge trapping but the standard deviation is almost identical in all cases. Like the data presented above the uniformly doped devices with just charge trapping in the oxide shows different behavior than the other three cases. In those two cases the average value of VT also moves to higher values when the trap concertation is increased. Fig. 7 shows the distributions of threshold voltage subject to a combination of VS and ITC for both two & three VSL NWTs.

Detailed simulation of SV and SR study of 5 nm NWT-based CMOS technology at 5nm is presented. Local variability sources including RDD, GER, WER and MGG are considered in this studying in addition to ITC. The presence of SV sources in the simulations affects dramatically the SR results.

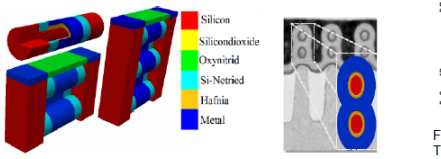

Fig. 1 (right) 3D schematic view a Si nanowire transistor (NTW) and material information for the two channel Si NWT(left), Cross-section TEM [1] image of two channel Si NWT.

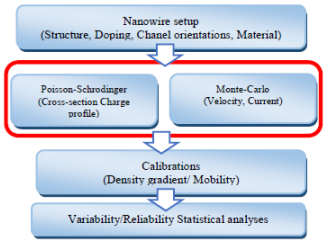

Fig 2: The simulation tool calibration flow chart

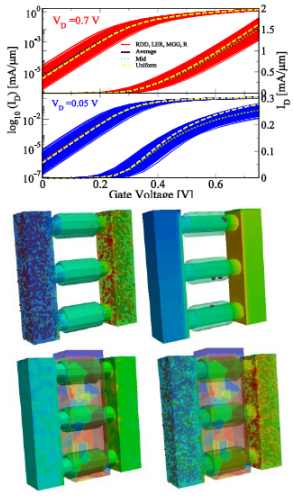

Fig. 3(top) Linear transfer characteristics for the ensemble with RDD, LER and MGG for double channel Si NWT at L_G=12 nm calibrated DD methods. (Bottom) 3D schematic of effects of SV and SR on the potential

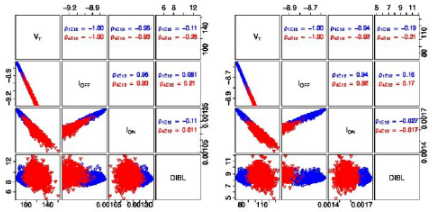

Fig. 4 Distribution of and correlations between extracted FOM from the TCAD simulations of individual ITC 1x10^{12} cm^{-1} and 4x10^{12} cm^{-1} for double NWT (left) and triple NWT (right).

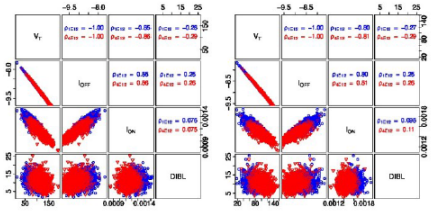

Fig. 5 Correlations between extracted FOM from the TCAD simulations for both ITC and VS effect (RDD, WER, MGG and R) for double NWT (left) and triple NWT (right).

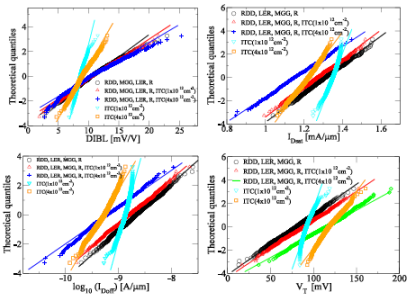

Fig. 6 Normal probability QQ-plot of DIBL, I_{lkad}, I_{off}, and V_T distributions due to individual VS effect of (RDD, LER, MGG, and R), and in their combination with 1x10^{12} cm^{-1} and 1x10^{12} cm^{-1} ITC .

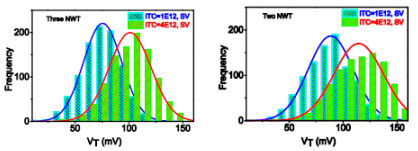

Fig. 7 Distributions of threshold voltage subject to VS effect of (RDD, LER, MGG, and R), and in their combination with 1x10^{12} cm^{-1} and 1x10^{12} cm^{-1} ITC 4x1012 cm-1 ITC for three VSL NWTs(left), and Two VSL NWT (right)

[1] H. Mertens et al., IEEE Symposium on VLSI Technology, 2016.
[2] A. Asenov et al, IEEE International Symposium on Quality Electronic Design (ISQED), 2016.
[3] T. Al-Ameri et al, IEEE Nanotechnology Materials and Devices Conference (NMDC). 2016.

Simulation of negative differential transconductance from devices fabricated using conventional CMOS technology

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Negative differential transconductance (NDT) has been recently observed in Si CMOS devices using lateral quantum wells defined by ion implantation[1]. Here, we present a theoretical study[2] of these unique type of devices, emphasizing the limitations of their practical realization as well of our understanding of the basic physical processes involved. At the same time, we also indicate possible future promising paths that can help to achieve and optimize the observed quantum behavior at room temperature.

The aforementioned CMOS (nMOS) de- vices have a lateral quantum well (QW) built into the surface channel, formed by reversing the dopant polarity of the shallow source/drain (S/D) extensions (pSDE) from the standard n-type (for an nMOS transistor) to p-type, as sketched in Fig. 1. A two- dimensional (2-D) QW is formed when the gate-to-source voltage V_{GS} is large enough to invert the channel. Electrons injected into the channel at energies equal to the bound states, created by the 2-D confinement, un- dergo resonant or sequential tunneling. At certain gate biases, when the energy of the bound states will coincide with the Fermi energy of the electrons in the source, the source-to-drain current, I_{DS}, should exhibit sharp peaks. This observation of NDT in the $I_{DS} - V_{GS}$ characteristics is the motivation behind our investigation.

The simulation of the device characteristics[2] is done in 2 steps. First, we solve the 2-D single electron 'effective mass' Luttinger-Kohn (Schrödinger) equation under *closed* boundary condition self-consistently with the Poisson equation[3] with a source- to-drain bias V_{DS} = 0 and for several values of V_{GS}. As a second step, ballistic electron transport via tunneling through the confined states is studied by solving the Schro¨ dinger equation with *open* boundary conditions (Quantum Transmitting Boundary Method)[4] using the self-consistent potential distribution obtained from the previous step. This allows us to calculate the current-voltage characteristics.

Figs. 2 and 3 show that the lateral QW nMOS devices exhibit the desired NDT at low temperatures (∼10 K) and for gate lengths of the order of 20 nm and smaller. The strong dependence of I_{DS} on temperature indicate a significant presence of thermionic emission over the pSDE barriers. Punch-through cur- rent is also observed in these devices. The energy spacing between the quasi bound states (Fig. 4) suggest that devices with a gate length of 10 nm and lower should ex- hibit a sharp NDT signature even at room temperature, provided an optimal design can be found that minimizes thermionic emission (requiring high pSDE barriers) and punch- through (that meets the opposite requirement of potential-barriers low enough to favor the tunneling current). The former plays a crucial role in suppressing the NDT, the latter is favored over the tunneling current for high pSDE barriers. We are currently looking into silicon-on-insulator (SOI) devices with high pSDE barriers that can meet the requirements to exhibit NDT at room temperature.