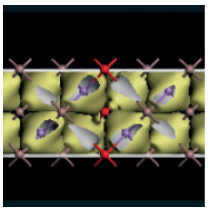

Metal grain work-function variability in GAA Si nanowire via a fluctuation sensitivity map

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One of the main burdens of a TCAD variability study of semiconductor devices is its high computational cost. There is a direct relation between the accuracy of results and the time needed to obtain them leading to substantial economic expenses. In this work, we present a technique to substantially reduce the computational costs when studying the impact of metal grain work-function variability (MGWV) on devices. The technique is based on a construction of a matrix, the fluctuation sensitivity map (FSM), with $M \times N$ elements ($FSM_{i,j}$), related to mesh points (u, v) on a metal gate. The FSM represents how sensitive V_T (or any other figure-of-merit) is to a work-function (WF), $WF(u, v)$, at that position in the gate. The construction of the FSM requires simulations of an ensemble of P device configurations. For the k-th device, a local sensitivity is:

$$FSM^k_{i,j} = \frac{\partial V^k_T}{\partial WF^k(f(i,j))} \qquad (1)$$

The residual of this equation is minimised by fitting coefficients a and b for each $(i;\ j)$ node using the relation:

$$V^k_T - \left(a(i,j) + b(i,j) \cdot WF^k(f(i,j))\right) = 0 \quad \forall k \in [1, P]$$

The value of each element of the matrix $FSM_{i,j}$ is equal to $b(i,j)$. The FSM can be used to predict the behaviour of a device for different grain sizes (GSs) using: i) a FSM for the device generated using a particular GS, ii) an ensemble of P realistic gate WF profiles, and iii) the standard deviation of the V_T ($\sigma V_T\ Real$) obtained after simulations of that ensemble of profiles. V_T can be estimated via the FSM ($V^K_T FSM$) as:

$$V^k_{T\ FSM} = \frac{1}{M \times N} \sum_{i,j}^{M,N} FSM_{ij} \times WF^k_{ij} \qquad (2)$$

There is a mismatch (α) between standard deviations of the real ($\sigma V_T\ Real$) and the FSM generated ($\sigma V_T\ FSM$) results, which is independent of the GS. Therefore:

$$\sigma(V_{T\ Predic}) = \alpha \times \sigma(V_{T\ FSM}) \simeq \sigma(V_{T\ Real}) \qquad (3)$$

As a test device, we investigate a 22 nm gate length Si

gate-all-around (GAA) nanowire (NW) FET that has been modelled from and calibrated to an experimental device [1], [2]. A schematic of the device can be seen in Fig. 1, and the calibration results in Fig. 2. A 3D density-gradient quantum- corrected drift-diffusion (DD-DG) simulator [3] is used while the TiN MGWV is modelled via the Voronoi approach [4].

Fig. 3 shows examples of work-function profiles that are wrapped around the gate, for four different grain sizes. Figs. 4 and 5 show 2D threshold voltage (VT) fluctuation sensitivity maps (FSM) for the GAA NW FET generated from Voronoi gate WF profiles (with either 7 or 10 nm GS) at low and high drain biases, respectively. The aggregated gate sensitivity (AGS) (shown at the bottom of the images) for a particular X-coordinate is computed as a normalised sum of all the VT values that form the column of the FSM associated to that coordinate. The largest sensitivity is found in the middle of the gate (X=0) when the drain bias is low

(0.05 V). At a high drain bias, the maximum slightly shifts towards the source end (X=−1.4 nm). However, the method used to calculate the FSM is affected by the GS. The larger the grain size, the less number of samples are needed to accurately capture the sensitivity of the gate region to the MGW variations. The lower the GS, the more affected the results will be by statistical noise. Once the ensemble of devices is simulated for a GS 10 nm (or any other chosen grain size) and the FSM is generated, it can be used to predict the VT variability for other GS, without further simulations saving a large amount of computational time. Fig. 6 shows scatter plots comparing the FSM generated VT distribution against the real one (from full simulations) for four different grain sizes. The predicted and full results are highly correlated (with Pearson correlation coefficients (r) equal to 0.93 or higher). Table I shows a comparison between σV_T due to the MGWV obtained from either full DD-DG simulations or the prediction by the FSM. Note that the % in the error of the prediction is lower than 7% in all the analysed GS. The execution time (Intel one-core i5-2500 processor at 3.3 GHz) is around 6 hr. Since we study 300 different configurations, the time to estimate $\sigma Real$ for the 4 analysed GS is $\sim$7200 hr. However, in the evaluation of $\sigma Predic$, we only need to simulate the ensemble of devices for the larger GS reducing the cost by a factor of 4, since the time needed to generate the FSM and to estimate the prediction is negligible (around 2 min).

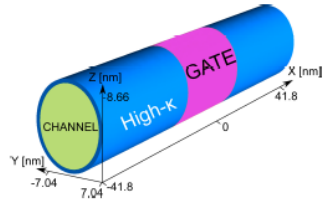

Fig. 1. Schematic of the 22 nm gate length Si GAA NW FET.

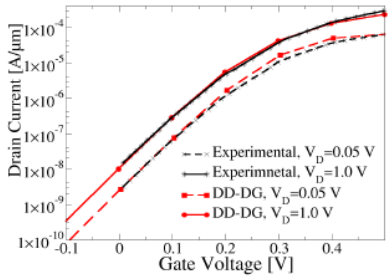

Fig. 2. I_D-VG for the 22 nm gate length Si GAA NW FET comparing experimental data against DD-DG results.

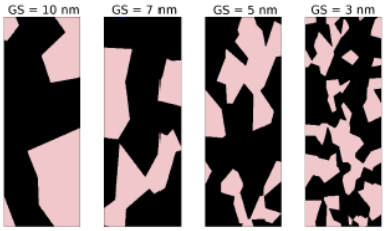

Fig. 3. Examples of TiN metal gate WF profiles generated using the Voronoi approach for four different GSs. The pink and black colours correspond to WFs of 4.4 and 4.6 eV, respectively.

TABLE I
THE V_T MGWV FOR THE 22 NM GATE LENGTH SI GAA NANOWIRE FET USING EITHER SIMULATION RESULTS (σ_{Real}) OR THE FSM MATRIX GENERATED FROM VORONOI PATCHES (σ_{Predic}) WITH A 10 NM GS. THE VALUE OF THE FITTING PARAMETER (α) AND THE PERCENTAGE OF ERROR OF THE FSM-BASED ESTIMATION ARE ALSO SHOWN.

α	GS (nm)	V_T (mV) σ_{Real}	V_T (mV) σ_{Predic}	Error %
9.6	10	36.70	36.70	0.0
	7	25.71	24.13	6.1
	5	18.41	17.99	2.2
	3	11.78	11.25	4.5

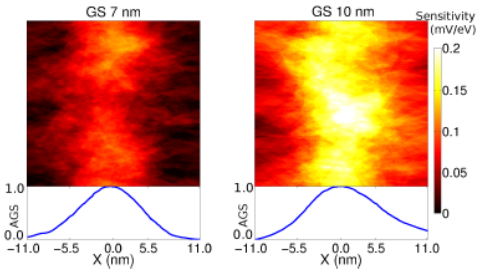

Fig. 4. 2D V_T FSMs for the 22 nm gate length Si GAA NW FET obtained via Voronoi gate WF profiles (top) and 1D AGS along the transport direction (bottom) at a drain bias of 0.05 V.

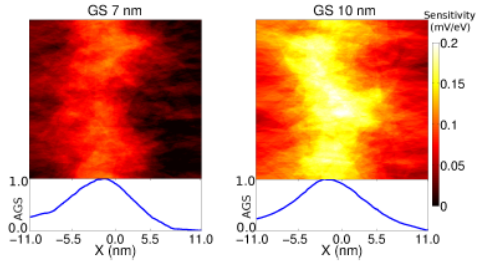

Fig. 5. 2D V_T FSMs for the 22 nm gate length Si GAA NW FET obtained via Voronoi gate WF profiles (top) and 1D AGS along the transport direction (bottom) at a drain bias of 1.0 V.

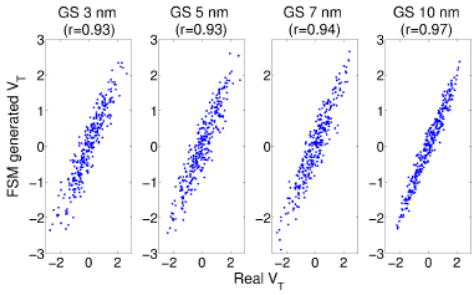

Fig. 6. Scatter plot of the predicted V_T distribution vs. the real one for four GSs at a drain bias of 1.0 V. The predicted values were obtained from a FSM generated from 300 Voronoi profiles with a 10 nm average GS and their corresponding V_T simulation values. V_T values were normalised to the mean value (set at 0) and the standard deviation (set at 1). The correlation coefficient (r) is shown for reference.

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