Inverse Modeling of Poly-Silicon in MOSFETs Using Quantum Mechanical Models

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1. Introduction

Performance degradation of a MOSFET caused by the depletion of a gate poly-silicon(poly-Si) is recognized as a serious problem as the gate oxide becomes thin. To accurately model the depletion of the gate poly-Si, it is very important to take the quantization effects into account not only in the inversion region but also in the accumulation region. In this paper, Schrödinger equations for both electrons and holes both in the gate poly-Si and silicon substrate were solved to reproduce full C-V characteristics of the poly-Si gate MOS structure. By the inverse modeling of several C-V characteristics discussed in recent studies has shown that there is a thin (10 to 15 [Å]) and low-concentration (about 1×10^{19} $[cm^{-3}]$) gap layer between the gate poly-Si and the gate oxide.

2. Simulation Models

The Schrödinger equations for electrons (Eqs. 1 and 2) and holes (Eqs. 3 and 4) were solved together with the Poisson equation (Eqs. 5 and 6). The Poisson equation was linearized by Pacelli's method.[1] To facilitate a continuous calculation from the inversion region to the accumulation region, both the quantized (2D) and the free (3D) carriers were taken into account as shown in Eqs. 7 - 10. The transition energies from the 2D to the 3D carriers ($E_{n\max}$ and $E_{p\max}$) were set up by a procedure proposed by Bowen et al..[2] To model the degeneration effect in the highly doped poly-Si region correctly, the modified Fermi-integrals (Eqs. 9 and 10) were numerically integrated and the bandgap narrowing effect (Eq. 11)[3] was also included. The sub-bands considered were the two- and the four-fold sub-bands for electrons and the heavy, the light and the split sub-bands for holes. The two lowest energy levels were taken into account in each sub-band.

$$\left[-\frac{\hbar^2}{2m_{nzi}}\frac{d^2}{dz^2}+E_C(z)\right]\Phi_{nij}(z)=E_{nij}\Phi_{nij}(z) \quad (1)$$

$$E_C(z)=-q\psi(z)+\frac{1}{2}E_g-\frac{1}{2}\Delta E_g\left(N_{DA}(z)\right) \quad (2)$$

$$\left[-\frac{\hbar^2}{2m_{pzi}}\frac{d^2}{dz^2}+E_V(z)\right]\Phi_{pij}(z)=E_{pij}\Phi_{pij}(z) \quad (3)$$

$$E_V(z)=-q\psi(z)-\frac{1}{2}E_g+\frac{1}{2}\Delta E_g\left(N_{DA}(z)\right)-\Delta E_{sp} \quad (4)$$

$$\frac{d^2}{dz^2}\psi(z)=-\frac{\rho(z)}{\epsilon_{Si}} \quad (5)$$

$$\begin{aligned}\rho(z) &= q\left(N_{DA}(z)\right. \\ &\quad \left.-n_{2D}(z)-n_{3D}(z)+p_{2D}(z)+p_{3D}(z)\right) \quad (6)\end{aligned}$$

$$\begin{aligned}n_{2D}(z) &= \sum_{i,j} D_{2ni}kT\left|\Phi_{nij}(z)\right|^2 \\ &\quad \left[\log\left\{1+\exp\left(\frac{E_F-E_{nij}}{kT}\right)\right\}\right. \\ &\quad \left.-\log\left\{1+\exp\left(\frac{E_F-E_{n\max}}{kT}\right)\right\}\right] \quad (7)\end{aligned}$$

$$\begin{aligned}p_{2D}(z) &= \sum_{i,j} D_{2pi}kT\left|\Phi_{pij}(z)\right|^2 \\ &\quad \left[\log\left\{1+\exp\left(\frac{E_{pij}-E_F}{kT}\right)\right\}\right. \\ &\quad \left.-\log\left\{1+\exp\left(\frac{E_{p\max}-E_F}{kT}\right)\right\}\right] \quad (8)\end{aligned}$$

$$\begin{aligned}n_{3D}(z) &= N_C\frac{2}{\sqrt{\pi}}\int_{\frac{E_{n\max}-E_C(z)}{kT}}^{\infty} \\ &\quad \frac{\sqrt{x}}{1+\exp\left(x-\frac{E_F-E_C(z)}{kT}\right)}dx \quad (9)\end{aligned}$$

$$\begin{aligned}p_{3D}(z) &= N_V\frac{2}{\sqrt{\pi}}\int_{\frac{E_V(z)-E_{p\max}}{kT}}^{\infty} \\ &\quad \frac{\sqrt{x}}{1+\exp\left(x-\frac{E_V(z)-E_F}{kT}\right)}dx \quad (10)\end{aligned}$$

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$$\Delta E_g\left(N_{DA}(z)\right) = qV_1\left[\log\left\{1+\left(\frac{|N_{DA}(z)|}{N_0}\right)^a\right\} - \log\left\{1+\left(\frac{|N_{DA}(z)|}{N_1}\right)^a\right\}\right] \quad (11)$$

Examples of the calculated carrier distribution of an nMOSFET in the strong inversion and accumulation conditions are shown in Figs. 1 and 2, respectively. Note that there is no quantization in the poly-Si accumulation layer in Fig. 2, because the potential dip is too narrow and shallow to confine the ground state.

3. Inverse Modeling

The C-V characteristics of nMOSFETs and pMOSFETs measured by Hu et al.[4] and Lee et al.[5] are compared with the simulation in Figs. 3 - 6. The oxide thicknesses and the doping concentrations in the silicon substrate were extracted so that the simulated results agree with the experiments respectively in the strong accumulation region and in the depletion region. The extracted values are summarized in Table I. It has been found that the oxide thicknesses electrically extracted in the strong accumulation condition are 5 – 6 [Å] thicker than the physical values. This is due to the quantization effect in the Si substrate region and also due to the degeneration (Fermi statistics) effect both in the Si substrate and poly-Si gate regions. In the figures, the dotted lines show the simulation results using the dopant concentrations in the poly-Si gate estimated in the respective studies. It has been found that all of the dotted lines overestimate the capacitances in the strong inversion regions although the gradients of the C-V curves there are almost the same as those in the experiments. This result suggests that the active dopant concentration around the poly-Si - SiO2 interface is smaller than the concentration in the bulk poly-Si. The solid lines in Figs. 3 - 6 show the simulation results when a thin (10 - 15 [Å]) and low-concentration (about 1×10^{19} $[cm^{-3}]$) gap layer is inserted between the gate poly-Si and the gate oxide as shown in Fig. 7 so that the C-V curves in the strong inversion region should agree with the experiments. The extracted gap layer thickness are also summarized in Table I. Note that the solution obtained by the inverse modeling is by no means unique and there are other possible combinations of thicknesses and the doping concentrations of the gap layer that can account for the experimental results. The electron distributions of the nMOSFET in [4] with and without a gap layer are compared in Fig. 8. In this case, the gap layer pushes out the depletion layer in the poly-Si gate by about 8 [Å].

4. Discussion

Since the gap layers exist both in the nMOSFETs and the pMOSFETs, this phenomenon seems to be related with the deactivation of the dopants occurred specifically at the poly-Si - SiO2 interface. The contribution of the gap layer to the total depletion layer width will become dominant as the doping level of the gate poly-Si becomes high. Therefore, for further improvement of the performance of the poly-Si gate MOSFET, the removal or the activation of the gap layer is necessary.

5. Conclusion

The inverse modeling of the gate poly-Si using quantum mechanical models both in the gate poly-Si and the substrate shows that there is a thin and low-concentration gap layer between the gate poly-Si and the gate oxide. For further improvement of the performance of the poly-Si gate MOSFET, the removal or the activation of the gap layer is required.

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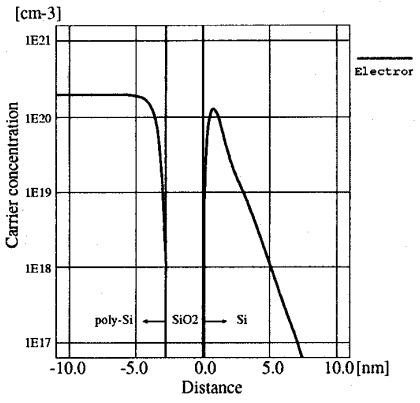

Fig. 1 : Example of the calculated carrier distribution of nMOS in the strong inversion condition (@ Vg = 3 [V]). The gate oxide thickness, substrate doping and poly-Si doping are 27.5 [Å], 3×10^{17} $[cm^{-3}]$ and 2×10^{20} $[cm^{-3}]$, respectively.

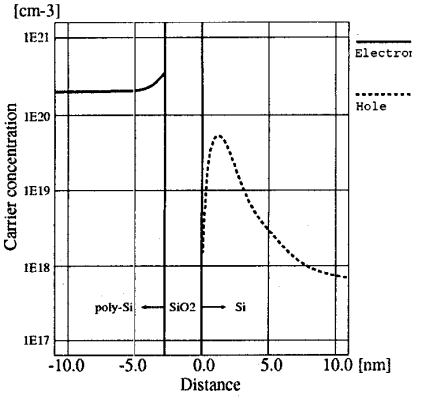

Fig. 2 : Example of the calculated carrier distribution of nMOS in the strong accumulation condition (@ Vg = -3 [V]). The gate oxide thickness, substrate doping and poly-Si doping are 27.5 [Å], 3×10^{17} $[cm^{-3}]$ and 2×10^{20} $[cm^{-3}]$, respectively. There is no quantization in the poly-Si accumulation layer because the potential dip is too narrow and shallow to confine the ground state.

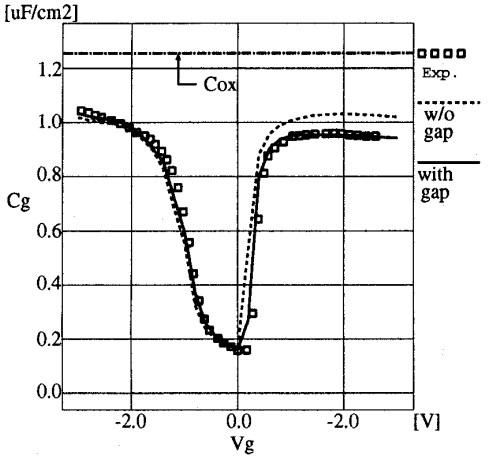

Fig. 3 : Simulated C-V curves and the experimental result of nMOS in [4], The extracted oxide thickness and substrate doping are respectively 27.5 [Å] (= electrically 33 [Å] @ Vg = -3 [V]) and 3×10^{17} $[cm^{-3}]$. The dotted line shows a simulation result using uniform poly-Si doping (2×10^{20} $[cm^{-3}]$) as evaluated in [4]. The solid line shows a simulation result assuming a gap layer (10 [Å], 1×10^{19} $[cm^{-3}]$) between the poly-Si and the gate oxide.

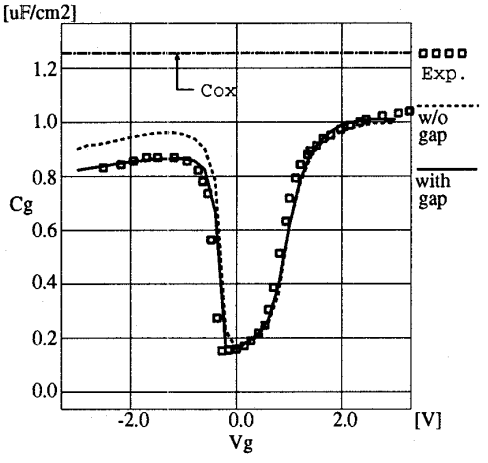

Fig. 4 : Simulated C-V curves and the experimental result of pMOS in [4], The extracted oxide thickness and substrate doping are respectively 27.5 [Å] (= electrically 33 [Å] @ Vg = +3 [V]) and 3×10^{17} $[cm^{-3}]$. The dotted line shows a simulation result using uniform poly-Si doping (8×10^{19} $[cm^{-3}]$) as evaluated in [4]. The solid line shows a simulation result assuming a gap layer (15 [Å], 1×10^{19} $[cm^{-3}]$) between the poly-Si and the gate oxide.

Table 1: Parameters extracted by the inverse modeling of the recent studies.

Source		T_{ox} [Å]		N_{sub} $[cm^{-3}]$	N_{poly} $[cm^{-3}]$	Gap layer [Å]
		Fabrication	Extraction	Extraction	Extraction	Extraction
Hu et al.[4]	nMOS	33 (@ Vg = -3 [V])	27.5	3×10^{17}	2×10^{20}	10
	pMOS	33 (@ Vg = +3 [V])	27.5	3×10^{17}	8×10^{19}	15
Lee et al.[5]	nMOS	47	45.5	5×10^{17}	2.7×10^{19}	15
	pMOS	47	48.5	4×10^{17}	6×10^{19}	15

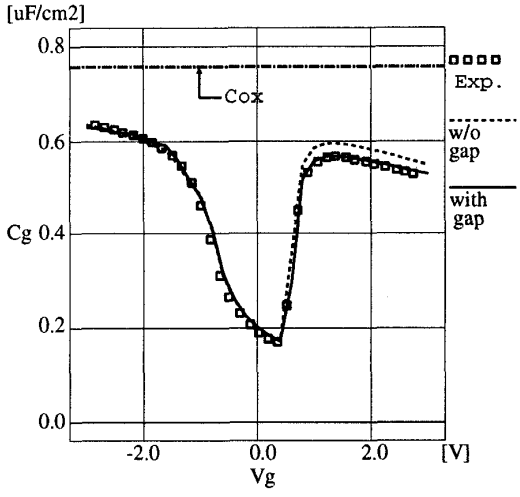

Fig. 5 : Simulated C-V curves and the experimental result of nMOS in [5], The extracted oxide thickness and substrate doping are respectively 45.5 [Å] (originally 47 [Å]) and 5×10^{17} $[cm^{-3}]$. The dotted line shows a simulation result using uniform poly-Si doping (2.7×10^{19} $[cm^{-3}]$) as evaluated in [5]. The solid line shows a simulation result assuming a gap layer (15 [Å], 1×10^{19} $[cm^{-3}]$) between the poly-Si and the gate oxide.

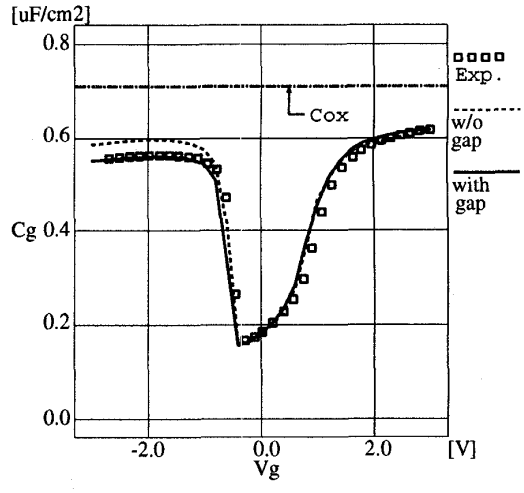

Fig. 6 : Simulated C-V curves and the experimental result of pMOS in [5], The extracted oxide thickness and substrate doping are respectively 48.5 [Å] (originally 47 [Å]) and 4×10^{17} $[cm^{-3}]$. The dotted line shows a simulation result using uniform poly-Si doping (6×10^{19} $[cm^{-3}]$) as evaluated in [5]. The solid line shows a simulation result assuming a gap layer (15 [Å], 1×10^{19} $[cm^{-3}]$) between the poly-Si and the gate oxide.

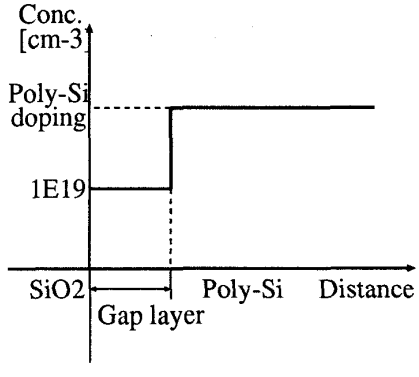

Fig. 7 : Schematic of the gap layer inserted between the gate poly-Si and the oxide. The doping concentration in the gap layer is assumed to be $1 \times 10^{19} cm^{-3}$ $[cm^{-3}]$ and its thickness is varied to reproduce the C-V characteristics in the strong inversion condition.

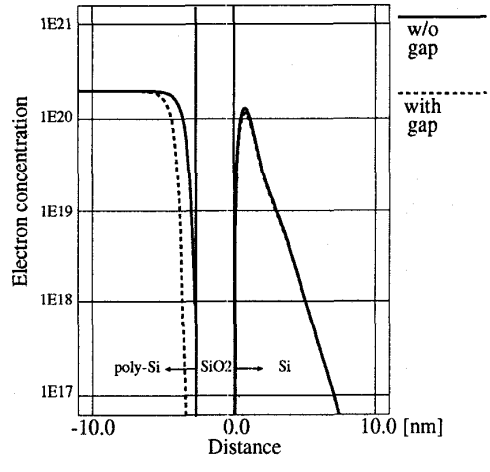

Fig. 8 : Electron distribution of the nMOS in [4] with (solid line) and without (dotted line) a gap layer. The applied gate voltage is 3 [V] (strong inversion). The gap layer pushes out the depletion layer in the poly-Si gate by about 8 [Å].