Simulation Analysis of Impurity Profile Extraction by SCM

K. Matsuzawa, Y. Oowaki, M. Nakamura[1], N. Aoki[2] and I. Mizushima[2]

Advanced Semiconductor Devices Research Laboratories, Toshiba Corporation
8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan
Phone: +81-45-770-3693, Fax: +81-45-770-3578,
E-mail: matsuzawa@amc.toshiba.co.jp

[1]Surface Science Laboratories, Toray Research Center, Inc.
[2]Microelectronics Engineering Laboratory, Toshiba Corporation

We investigate the propriety of SCM (scanning capacitance microscopy) for determination of impurity distribution of MOSFET. Two-dimensional impurity distribution is converted from $\Delta C/\Delta V$ signal obtained by SCM. It is revealed that the SCM signal is quite sensitive to the effects of charge depletion around pn junction, singularity of structure in vicinity of SiO_2/Si interface (edge effect), and the work function of the gate electrode. Making use of process/device simulations to analyze these effects, it is found that the SCM signal near channel surface region of Si substrate contains large error due to the edge effects. The lateral extent of the source/drain region obtained by SCM shows reasonable agreement with that determined by measurements and simulations of electrical characteristics of MOSFET.

1. Introduction

SCM has widely been recognized as an effective tool for the two-dimensional (2D) impurity profiling [1]-[5]. Junction delineation was performed below the channel length less than 0.1 μm [6]. However, the 2D profiling on the total area on MOSFETs has not yet succeeded because of the difficult interpretation of SCM signals affected by the impurity distribution and structure of samples. The purpose of this paper is to clarify these effects on the 2D profiling of MOSFETs by measurements and process/device simulations.

In following section, the SCM measurement of an n-MOSFET is described. In section 3, a depth profile in the source/drain (S/D) region obtained from SCM signals is evaluated by the comparison with SIMS profile, and unexpected peaks observed at the SiO_2/Si interface and pn junction in SCM results are explained by the three-dimensional (3D) device simulation of the SCM itself. In section 4, it is shown that the SCM signals at the channel surface are enormously modulated by an edge effect and the work function of the gate electrode. In section 5, the lateral extent of S/D n^+ region obtained from the SCM signals is examined by the electrical measurements of MOSFET characteristics and process/device simulations. In section 6, conclusions and suggestions for SCM measurements are included.

2. SCM Measurements

The 2D impurity profile of the nMOSFET (single S/D, L=1 μm, t_{ox}=20 nm, x_j=0.1 μm, n^+ poly gate) was obtained by SCM measurements. The measurement conditions are the frequency of 100 kHz, the offset voltage of 0 V, the measurement area of 1.6 μm $\times$ 1.6 μm, and the measurement points of 256 $\times$ 256. The SCM signals are converted to impurity concentrations by Eqn. (1) based on the absolute depletion approximation:

$$N = N_0\left(\frac{C_{ox}}{\Delta C} - 1\right)^2, \qquad (1)$$

where N is the impurity concentration, C_{ox} the capacitance between the tip and the sample, and N_0 the reference concentration. N_0 and C_{ox} in Eqn. (1) are determined by two different concentrations known by SIMS. The SCM signal is proportional to ΔC. It is ideal to extract the impurity profile inversely from SCM signals by using device simulations. However, the simulation of 2D impurity profile from SCM signals requires full 3D calculations including 3D structure of the system, namely topology of scanning tip, and physical and electrical structure of native oxide on the sample. Therefore, we have adopted the simple method and include uncertain

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factors in N_0 and C_{ox} by fitting them to SIMS results.

3. Depth Profile in S/D region

Figure 1 shows the depth distribution of SCM signals in the S/D region, and Fig. 2 shows that the impurity profile calculated from SCM signals using Eqn. (1) gives good agreement with SIMS profiles. However, two peaks are observed in SCM results. The peak at the SiO_2/Si interface (y=0) is due to the edge effect, which is caused by volume reduction of the depletion region formed by the tip at the substrate edge, resulting in reduction in ΔC and enhancement of N through Eqn. (1). The other peak reflects the carrier reduction in the depletion region formed by the pn junction. These effects have been verified by simulations of SCM itself using the 3D device simulator DIAMOND, as shown in Fig. 3. It should be noted that the exact shape of the tip and the exact thickness of the native oxide are unknown. Therefore, the interpretation using 3D device simulation results must be qualitative in this work. In the SCM simulation, the thickness of native oxide is 1 nm, and the tip is treated as a plate with the same area of $(1.6\ \mu m/256)^2$ as one pixel of SCM measurements.

4. Channel Profile

Figure 4 is the impurity profile obtained from SCM signals using Eqn. (1). The impurity concentration at the channel surface is expected to be about 10^{17} cm^{-3} according to SIMS and the process simulator TOPAZ. However, SCM results show extremely high impurity concentration in the channel region, which is caused by not only the edge effect but also the work function of the gate electrode. Namely, the charge depletion by the built-in potential between n^+ poly-Si-gate and p-type substrate causes the reduction of SCM signals even at the zero bias condition, resulting in the overestimation of the impurity concentration at the channel surface through Eqn. (1). The reduction of SCM signals could be suppressed by the gate bias of the flat band voltage, as has been verified by 3D SCM simulations, shown in Fig. 5. However, the edge effect remains. Actually, it is difficult to extract the channel surface concentration by biasing the gate to cancel the built-in potential in the case where the SCM signals become lower than measurement sensitivity due to the edge effect. This problem could be solved by the offset bias control as well as the gate bias.

5. Lateral Profile of S/D

It is difficult to know the lateral extent of the S/D n^+ region at just channel surface (y=0) due to the edge effect and the work function of the gate electrode as pointed out in previous sections. Therefore, the lateral extent has be deduced at a position slightly deeper (y=18.8 nm) from the channel surface, where the influence of the edge effect and the work function decrease. The difference between the lateral extent of SCM and the result of TOPAZ, referred to as δL, is consistent with the difference between

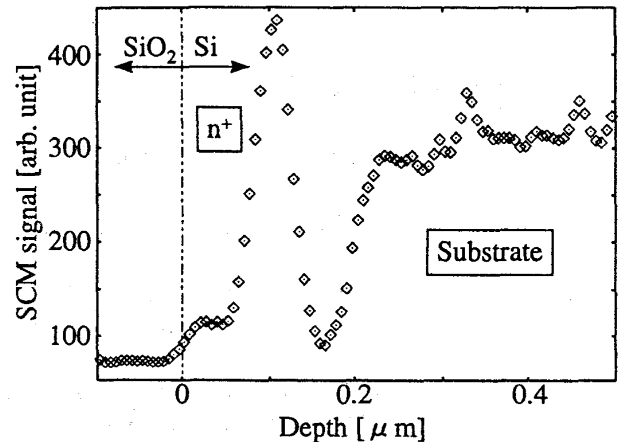

Figure 1: SCM signals along depth direction in n^+ region of nMOSFET.

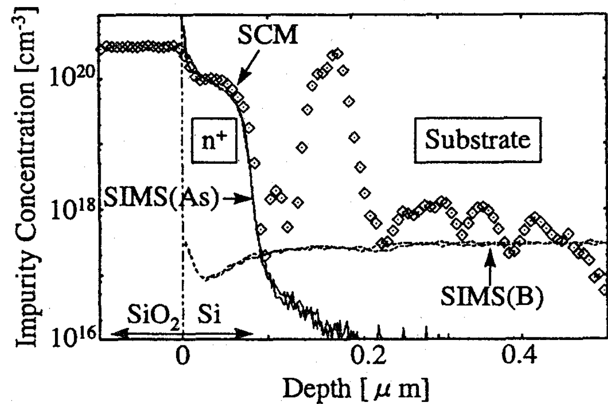

Figure 2: Comparison of impurity profiles along depth direction in n^+ region between SCM and SIMS.

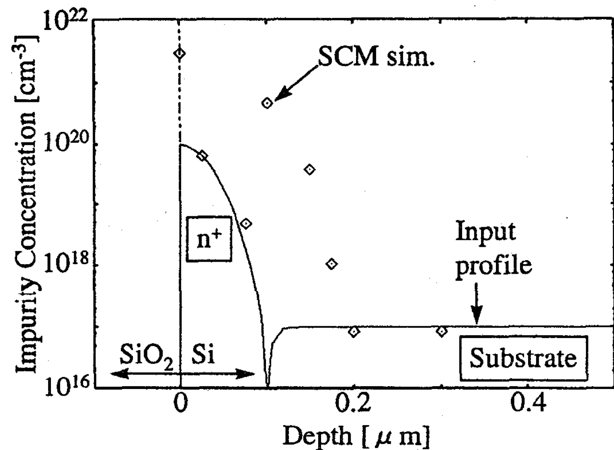

Figure 3: Comparison of SCM simulations with input impurity profile.

measurements and simulations in the gate shortening ΔL defined by Terada's method [7]. Figure 6 shows the gate bias dependence of ΔL, which reflects the lateral diffusion of the n^+ region. The difference in ΔL between measurements and simulations under the high gate voltages is almost the same as the δL shown in Fig. 4. Consequently, the lateral extent of S/D region deduced from SCM signals seems to be reasonable, even though the channel profile extracted from SCM signals is modulated.

In Fig. 6, the discrepancy between measurements and simulations in the gate bias dependence of ΔL is observed under the low gate bias. It could be explained by considering the modulation of the channel profile by D-ED (damage enhanced diffusion) near the S/D region, or the tail diffusion of the S/D impurity, which affect ΔL under low gate bias conditions. On the other hand, under high gate bias conditions, such effects are diminished, because the concentration of inversion electrons is sufficiently higher than the modulated impurity concentration around the channel surface near the S/D region. Consequently, δL shown in Fig. 4 should be compared with δL by Terada's method under the high gate bias conditions to eliminate uncertainty due to the modulation of the impurity concentration near the S/D region.

6. Conclusions

2D impurity profiling by SCM has been examined by measurements and simulations. The profile along the depth direction and the lateral extent of the S/D region can be deduced from SCM. However, the SCM signals are modulated by the edge effect, the charge depletion around pn junction, and the work function of the gate electrode. SCM could allow the more detailed profile at the channel surface with the bias control and the 3D device simulations, including the shapes of tips as well as structures of samples.

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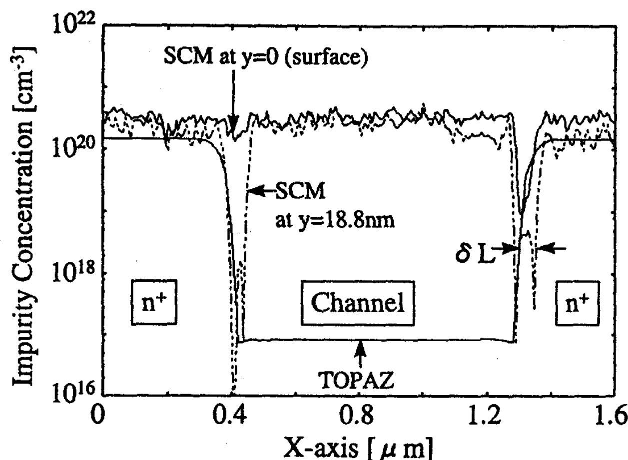

Figure 4: Impurity profiles along channel surface obtained by SCM and TOPAZ.

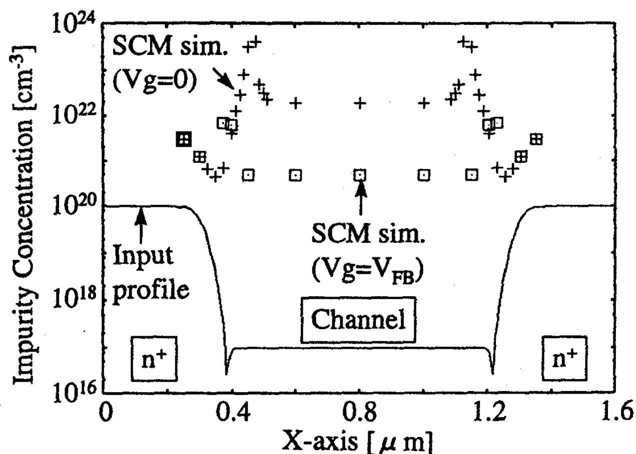

Figure 5: Impurity profile along channel surface obtained by 3D SCM simulation.

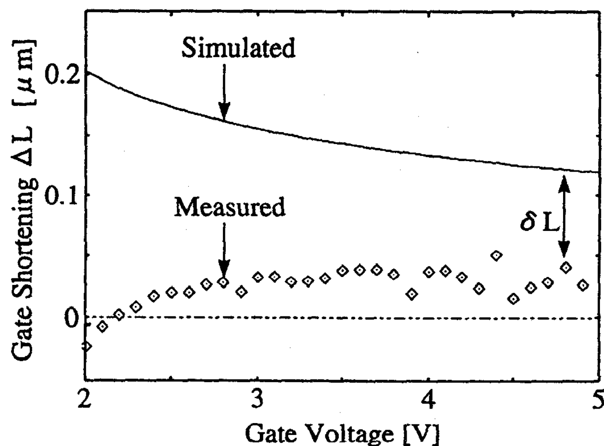

Figure 6: Dependence of gate shortening ΔL on gate voltage.