# Enhancement of Weak Impact Ionization in InAlAs/InGaAs HEMTs Induced by Surface Traps: Simulation and Experiments

Tetsuya Suemitsu*, Masaaki Tomizawa, Takatomo Enoki, and Yasunobu Ishii
*NTT System Electronics Laboratories*
*3-1 Morinosato Wakamiya, Atsugi, Kanagawa 243-0198, Japan*
* Phone: +81-462-40-2795 Fax: +81-462-40-2872 E-mail: sue@aecl.ntt.co.jp

## 1. Introduction

InGaAs and InAlAs are lattice-matched to InP substrate at an indium (In) content of 53% and 52%, respectively. The large In content provides a small effective mass for two-dimensional electron gas (2DEG) in InGaAs. In addition, a large conduction band discontinuity between InAlAs and InGaAs can achieve high 2DEG density. Hence this material system leads to excellent RF performance in the HEMTs. For example, 0.1-μm-gate InAlAs/InGaAs HEMTs can achieve a cutoff frequency ($f_T$) of over 200 GHz, and $f_T$ > 300 GHz has also been reported with a gate length of 50 nm [1-3]. These are the promising devices for high-speed digital ICs and high-frequency monolithic ICs for communication and sensor systems [4].

The small bandgap for InGaAs lattice-matched to InP (0.76 eV), however, causes problems with respect to impact ionization. The kink phenomena - the anomalous increase in drain current - is considered to be one of those problems [5]. We have modeled the kink by the hole pile-up and surface traps in the source-gate recess region adjacent to the gate [6,7]. Figure 1 shows the schematic structure of the InP-based HEMTs. Undoped free surface is exposed in the recess region adjacent to the gate electrode. Surface traps in the recess region, represented by deep acceptors in our model, are responsible for the Fermi level pinning. The proposed model of the kink is illustrated in Fig. 2. Holes generated by impact ionization accumulate in the source side of the HEMTs. Since the potential barrier for holes is small, some of the holes move into the surface depletion region. The resulting modulation of the potential profile leads to an increase in the electron density in the recess region and the drain current. Hence the surface traps in the source-gate recess region plays an important role on the kink. The model is supported by recent experiments which shows that the behavior of the kink significantly depends on the surface material in the recess region [8]. In this model, the effect of the surface traps in the gate-drain recess region is not clarified yet despite its role on the kink is pointed out [9]. In this paper, we report the results showing that the surface traps in the gate-drain recess region enhance the weak impact ionization at low biases. The simulation results agree well with the change in the output characteristics by means of hot-electron degradation tests carried out on the InP-based HEMTs.

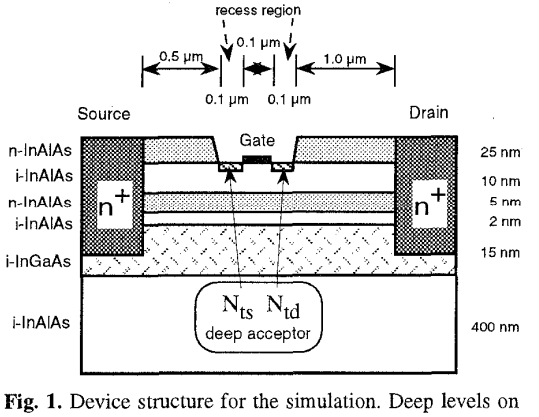


**Fig. 1.** Device structure for the simulation. Deep levels on the recess region represent the surface traps.

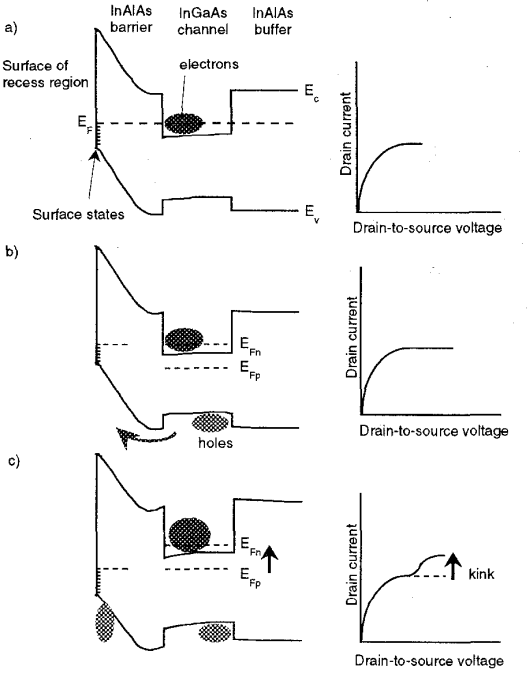


**Fig. 2.** Proposed mechanism of the kink. In source-gate recess region, (a) Quasi-Fermi levels for electron ($E_{Fn}$) and holes ($E_{Fp}$) are equal at low $V_{ds}$. (b) When holes begin to accumulate, $E_{Fp}$ in the channel moves closer to valence band. (c) Some of the holes move to the surface depletion region to equalize $E_{Fp}$, resulting in an increase in channel electron density.

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## 2. Device Modeling

Figure 1 shows the simulated device structure. The uncapped region beside the gate electrode represents the recess groove at the gate periphery. Although this recess region is usually much smaller than the capped region, small electron density due to the lack of the cap layer causes substantial parasitic resistance. The modeling of the recess region is therefore important for accurate simulation. In this study, a deep-acceptor is embedded on the surface of the recess region to represent the surface traps. The energy level of the deep acceptor is assumed to be 0.28 eV above the valence band edge, which was fitted so as to provide realistic I-V characteristics. The carrier transport is described by the drift diffusion model [10]. Electron- and hole-initiated impact ionization are taken into account. Non-local effect plays an important role on the impact ionization in submicron gate FETs because the high-field region is confined over a small distance between the gate and the drain. The impact ionization is therefore described by the effective carrier temperature model based on the energy balance equation [11,12]: The carrier temperature ($T$) is obtained by solving the energy balance equation

$$\mathrm{div}\left(\frac{5}{2}k_B n \boldsymbol{v} T\right) = -qn\boldsymbol{v}\cdot\boldsymbol{F} - \frac{3}{2}k_B n\frac{T-T_0}{\tau} \quad , \qquad (1)$$

where $n$ is the carrier density, $\boldsymbol{v}$ is the drift velocity, $\tau$ is the energy relaxation time, $\mathbf{F}$ is the electric field, and $T_0$ is the lattice temperature. The ionization coefficient $\alpha$ is calculated using $T$ as

$$\alpha = A\exp\left(-\frac{E}{k_B(T-T_0)}\right), \qquad (2)$$

where $A$ and $E$ are material-dependent parameters. If the electric field is uniform, $\alpha$ is given by a local field value, i.e.,

$$\alpha = A\exp(-B/F), \qquad (3)$$

and the energy gained from the field is given by $\frac{3}{2}k_B(T-T_0) = \tau v_s F$, where $v_s$ is the saturation velocity of the carriers. By comparing the above expression for $\alpha$, $E$ is given by $E = \frac{2}{3}\tau v_s B$. Here, $A$ and $B$ can be determined experimentally by the measurements of collector multiplication in HBTs or by the photo-current gain in photo diodes [13]. With regard to $In_{0.53}Ga_{0.47}As$, $A$ = 8.6 x $10^6$ $cm^{-1}$and $B$ = 3.5 x $10^6$ V/cm for electrons and $A$ = 2.3 x $10^7$ $cm^{-1}$and $B$ = 4.5 x $10^6$ V/cm for holes. The energy relaxation time ($\tau$) and the recombination lifetime are assumed to be 250 fs and 1 ns, respectively. The generation rate of electron-hole pairs for each mesh point $G(x,y)$ is calculated by

$$qG(x,y) = \alpha J_n(x,y) + \beta J_p(x,y),$$

where $\alpha$ ($\beta$) is electron (hole) initiated impact ionization coefficient, and $J_n$ ($J_p$) are the electron (hole) current density.

The impact of the non-local effects is observed in the simulation results. Figure 3 shows the generation rate for electron-hole pairs (by impact ionization) $G$ in the HEMT, i.e., $G = \int_{\text{device}} G(x,y)dxdy$ as a function of the drain bias

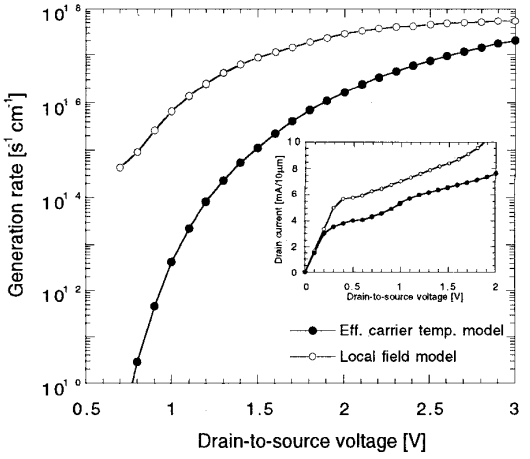


**Fig. 3.** Generation rate of electron-hole pairs simulated using the effective carrier temperature model and the local field model. (inset) Simulated I-V characteristics for both models.

($V_{ds}$) for the effective carrier temperature model, eqs. (1) and (2), and the local field model, eq. (3). The generation rate calculated by the effective carrier temperature model increases rapidly at around $V_{ds}$ = 0.8 V, which means that the average energy of the carriers exceeds the threshold of the impact ionization. In the local field model, on the other hand, there is no significant increase in $G$ reflecting the threshold energy and $G$ is overestimated especially in low biases. The inset in Fig. 3 shows the simulated I-V characteristics for both models. The local field model fails to represent the kink due to the overestimation of the impact ionization and resulting hole concentration at low $V_{ds}$.

## 3. Results and Discussions

In order to ascertain the role of the surface traps in the kink phenomena, the simulation was carried out by changing the surface-trap densities in the recess region in source-gate ($N_{ts}$) and gate-drain ($N_{td}$). Figure 4(a) shows the I-V characteristics with various $N_{ts}$. The saturation current decreases and the kink becomes more significant with increasing $N_{ts}$. The decrease in the saturation current is attributed to the surface-trap-induced reduction of electron density, and the reduced electron density is enhanced by the pile-up of holes, resulting in the kink [6,7] as shown in Fig. 2. Figure 4(b) shows the change in I-V curves with $N_{td}$. In contrast to the former case, the saturation current at high drain voltage ($V_{ds}$) is not changed by $N_{td}$, but the collapse of the drain current ($I_d$) at low $V_{ds}$ becomes significant with increasing $N_{td}$. Another feature that should be pointed is that the bias at which the kink appears ($V_{kink}$) shifts toward low $V_{ds}$. This result indicates that the surface traps at the drain side also have an influence on the

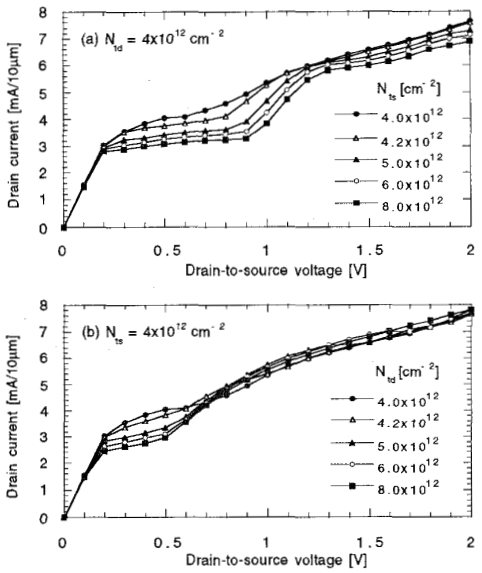


**Fig. 4.** Simulated I-V characteristics with various combinations of surface trap densities in the source-gate ($N_{ts}$) and gate-drain ($N_{td}$) recess regions. (a) $N_{ts}$ dependence and (b) $N_{td}$ dependence of I-V curves. Gate voltage ($V_{gs}$) is 0.1 V.

kink.

The simulation results are compared to the results of the hot-electron degradation tests [9]. The samples are 0.1-μm-gate InAlAs/InGaAs HEMTs lattice-matched to InP substrates. The epitaxial structure was grown by molecular beam epitaxy and consists of, from bottom to top, 200-nm InAlAs buffer, 15-nm InGaAs channel, 2-nm InAlAs spacer, 5-nm Si-doped InAlAs (1 x 10$^{19}$ cm$^{-3}$), 20-nm InAlAs barrier, and n$^{+}$-doped InGaAs/InAlAs cap layers. Details of the fabrication process is reported elsewhere [2]. The gate metal (Ti/Pt/Au) was evaporated on the InAlAs barrier after removing the cap layers by wet-chemical etching. The bias stress was applied to the samples at room temperature. Figure 5 shows the typical I-V characteristics of the HEMT. The kink is small under the initial condition. After a long-term bias stress is applied, however, the degradation of $I_d$ is observed; a notable feature is that the kink becomes larger and $V_{kink}$ shifts to the lower $V_{ds}$. This result can be explained by the simulation results. The hot-electron stress enhances the surface trap density mainly in the gate-drain recess region. The shift in $V_{kink}$ is attributed to the increase in the surface trap density in the gate-drain recess region as shown in Fig. 4(b). The decrease in the saturation current at high $V_{ds}$ observed in Fig. 5 can be explained by increased surface traps in the source-gate recess region caused by non-zero gate bias during the stress.

To clarify the mechanism behind the shift in $V_{kink}$, we calculated the generation rate for electron-hole pairs $G$. Figure 6 shows $G$ as a function of the inverse of the drain-to-gate voltage ($1/V_{dg}$). At low $1/V_{dg}$ (i.e., high $V_{dg}$), the generation rate is independent of $N_{td}$. At high $1/V_{dg}$ (low $V_{dg}$), however, it increases with $N_{td}$ significantly. This means that the surface traps in the gate-drain recess region increase the weak impact ionization at low biases. Figure 7 shows the potential profile in the channel under the gate. The large $N_{td}$ suppresses the voltage drop in the source-gate recess region and enhances the drop at the drain side. These results indicate that the surface traps in the gate-drain recess region enlarge the voltage drop there and, as a result, the weak impact ionization is enhanced. The enhanced impact ionization and resulting increased hole density in the source-gate recess region at low $V_{dg}$ are the reasons for the change in the shift in $V_{kink}$. The change in the potential profile is understood as follows: Since the lack of the cap layer and the existence of the surface traps reduce the carrier density in both source-gate and gate-drain recess regions, the potential drop mainly occurs in both recess regions at low $V_{dg}$. As $N_{td}$ becomes larger than $N_{ts}$, the number of electrons in the gate-drain recess region decreases. This leads to a larger potential drop in the gate-drain recess region. The $N_{td}$ dependence of the potential profile is, however, eliminated at high $V_{dg}$ because the applied voltage forms a drain

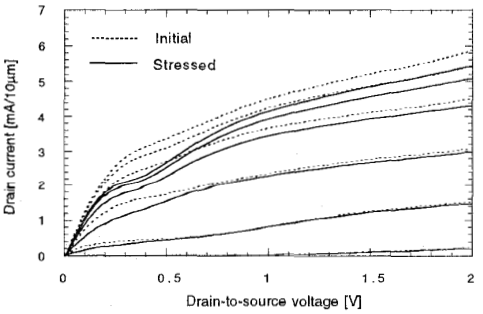


**Fig. 5.** Experimental I-V characteristics of an InP-based InAlAs/InGaAs HEMT before and after 52-h bias stress. $V_{gs}$ is changed from 0.1 to -0.9 V in 0.2 V steps. The stress condition is $V_{ds}$ = 3.5 V and $V_{gs}$ = -0.96 V.

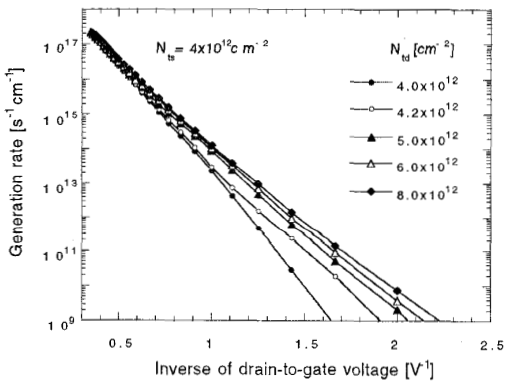


**Fig. 6.** Generation rate of electron-hole pairs due to impact ionization as a function of the inverse of the drain-to-gate voltage ($1/V_{dg}$).

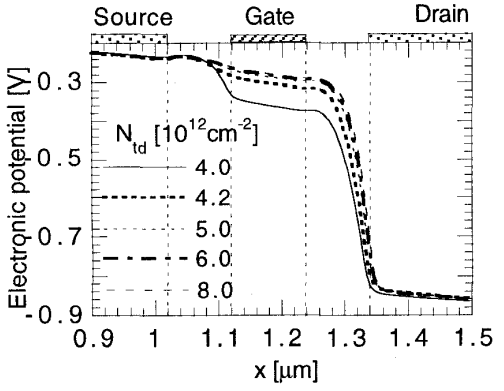


**Fig. 7.** Potential profile in the channel layer (distance from barrier/channel interface: 5.5 nm) under the gate region. $V_{gs}$ = 0.1 V, $V_{ds}$ = 0.8 V, and $N_{ts} = 4\text{x}10^{12}$ cm$^{-2}$.

depletion region and it overrides the surface-trap-induced carrier depletion in the gate-drain recess region. Therefore, the impact ionization rate is independent of $N_{td}$ at high $V_{dg}$ as shown in Fig. 6.

## 4. Conclusions

The correlation among the impact ionization, the surface traps, and the drain current degradation (kink) has been studied. The two-dimensional device simulation reveals that the increase in the surface traps at the recess region between gate and drain causes an enhancement of the weak impact ionization at low biases. This is one of the possible reasons for the kink phenomenon associated with hot-electron-induced degradation.

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