Understanding Conductance Quantization in Thin SOI MOSFET by Quantized-Energy-Level Simulation

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Abstracts

A device simulator to investigate conductance oscillations in small scale devices is developed. The simulator is applied to analyze measured transconductance g_m oscillations of a thin Silicon-On-Insulator (SOI) MOSFET. It is explained that the oscillations are caused by thin Si-layer region in the channel, about 15 % thinner, originated by roughness at the interface between the Si and buried SiO_2. The thinner region affects as a barrier for carriers. Transmission of the carriers at the ground state through the barrier is mainly responsible for the g_m oscillations in the gate voltage region V_G above the threshold condition. For larger V_G values the first-excited state becomes important.

1. Introduction

Figure 1 shows measured drain current I_D versus V_G for a SOI-MOSFET at 39 K. Device parameters of the MOSFET are summarized in Table 1 [1]. There are clear oscillations of I_D in the sub-threshold region. Even above the threshold region clear oscillations are observed in the transconductance g_m. The oscillations have been qualitatively reproduced by considering both the vertical and the lateral quantizations in the channel [2]. Thin active Si-layer is responsible for the former, and terrace structure of the Si/SiO_2 interface is for the latter. Here, a device simulator developed for studying such quantized devices will be demonstrated. Calculated oscillations are investigated to determine microscopic structure of the device.

2. Methods

2.1 Modeling Procedure

Figure 2 shows schematic of a studied SOI-MOSFET with device parameters given in Table 1. The active Si-layer thickness t_{si} is only 6 nm. A terrace structure at the interface between the Si/buried SiO_2 has been observed by an AFM picture. The average height of the terrace is estimated to be about 0.5 nm with the periodicity of 100 nm.

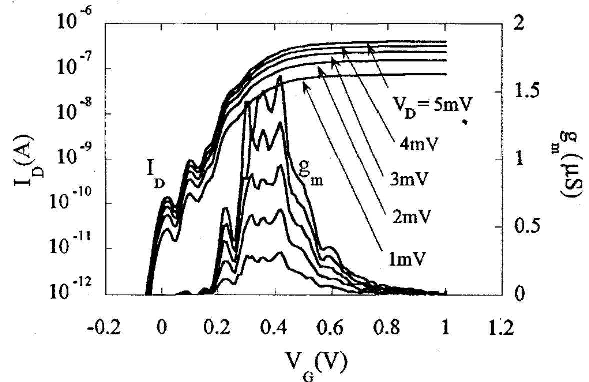

Fig. 1: Measured I_D and g_m as a function of V_G at 39 K. There are I_D oscillations in sub-threshold region and there are g_m oscillations above the threshold.

For modeling the terrace structure is simplified by a step function as shown in Fig. 3. Here two different thicknesses of the active Si-layer t_{si} are distinguished. The thicker thickness t_{si1} is 6 nm and the thinner one t_{si2} is 5 nm. The different thicknesses result in different quantized energy levels along the depth direction. The different energy levels affect as a barrier for carriers along the channel. The large difference in t_{si} causes the high barrier height. The energy levels are calculated by solving the Poisson equation and the Schrödinger equation simultaniously.

The energy difference V_0 between the two different t_{si} values (see Fig. 3) is used to calculate the transmission probability of carriers on each energy level. For the calculation the barrier width d is an important parameter in addition to the height V_0.

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Table 1: Device parameters of the fabricated SOI-MOSFETs.

Gate-Oxide Thickness : t_{ox}	3 nm
Silicon Layer Thickness : t_{si}	6 nm
buried-Oxide Thickness : t_{box}	100 nm
Channel Length : L_{ch}	50 nm
Substrate Concentration : N_A	1.0×10^{16} cm^{-3}
S/D Concentration : N_D	2.0×10^{20} cm^{-3}

2.2 Calculation Procedure

The flowchart of a simulator devloped is shown in Fig. 4. It consists of three parts. The first part (I) calculates I_D for a given V_G value. We solve the Poisson equation

$$\frac{d^2\phi}{dx^2} = -\frac{q}{\epsilon_s}\left\{p_{p0}\left(e^{-\beta\phi}-1\right) - n_{p0}\left(e^{\beta\phi}-1\right)\right\} \quad (1)$$

where ϕ, q, ϵ_s, n_{p0}, p_{p0} and β are the potential value, elementaly charge, parmittivity of Si, electron density, hole density and $\beta \equiv q/kT$, respectively. With use of the calculated ϕ the drift-diffusion equation is solved under the charge sheet approximation. This part of calculation doesn't include the quantization effect, and can be replaced by a hydrodynamic simulation to secure device physics for reduced device sizes.

The second part (II) calculates quantized energy levels in the vertical direction self-consistently [3]. With use of the potential distribution solved in the first part, the Schrödinger equation

$$\left\{-\frac{\hbar^2}{2m_j}\frac{d^2}{dx^2} + q\phi\right\}\psi_{ij} = E_{ij}\psi_{ij} \quad (2)$$

is solved, where $\hbar$, ψ_{ij} and E_{ij} are reduced Planck constant, wave function and quantized energy, respectively. For this calculation, we take into account two modes of effective electron masses m_j (longitudinal and transverse) destinguished by j in equation (2). The calculated ϕ, ψ_{ij} and E_{ij} are used as initial values for the following self-consistent calculation. After calculating the Fermi-energy, the Poisson equation including the quantization effect is solved .

$$\frac{d^2\phi}{dx^2} = -\frac{1}{\epsilon_s}\left(\rho_{dep} - q\sum_{j=1}^{2}\sum_{i=0}^{\infty} N_{ij}\psi_{ij}^2\right) \quad (3)$$

$$N_{ij} = \frac{n_{vj} m_{dj} k_B T}{\pi\hbar^2}\ln\left\{1+\exp\left(-\frac{E_F - E_{ij}}{k_B T}\right)\right\}. \quad (4)$$

The Schrödinger equation is solved with the calculated ϕ including the quantization effect. Because of the terrace structure at the Si/buried SiO_2 interface (depicted schematically in Fig. 3), the whole calculation of the part II in Fig. 4 has to be repeated twice to calculate the energy levels for two different t_{si} values.

The third part (III) calculates the transmission probability between two different quantized energy levels in the channel caused by the Si-layer thickness variation along the channel [4]. The transmission probability is calculated as

$$T_r = \left|\frac{e^{-ik_1 d}}{\cos(k_2 d) + i(\epsilon/2)\sin(k_2 d)}\right|^2 \quad (5)$$

$$\epsilon = \frac{k_2}{k_1} + \frac{k_1}{k_2}, \quad (6)$$

where k_1 and k_2 are the wave vector at the position A and the position B. Calculated carrier density for each energy level of the second part (II) is multiplied by this transmission probability for each energy level. To calculate I_D mobility value of carriers is required. It is estimated from measured I_D for each V_G value with use of the calculated carrier density in the first part (I). The mobility value is approximated to be the same for all energy levels. Finally the transconductance g_m for each energy lvel is calculated by differentiating I_D with respect to V_G.

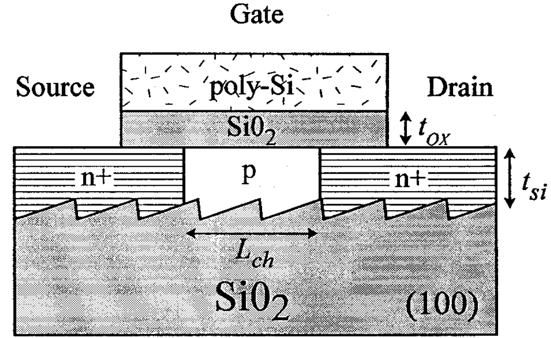

Fig. 2: Schematic picture of SOI MOSFET.

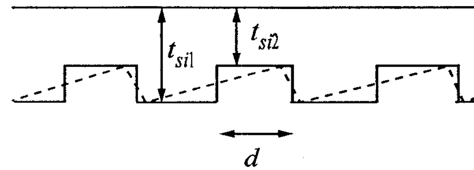

Fig. 3: Schematic diagram for modeling the terrace structure of SOI. Two Si-layer thicknesses, t_{si1} and t_{si2}, are introduced.

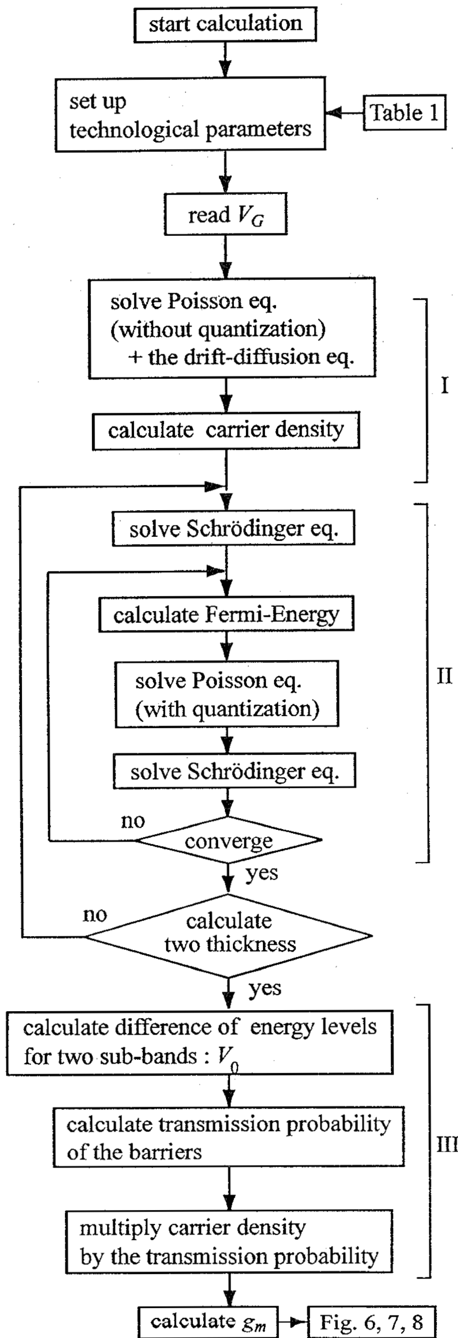

Fig. 4: Flowchart of our over all simulator.

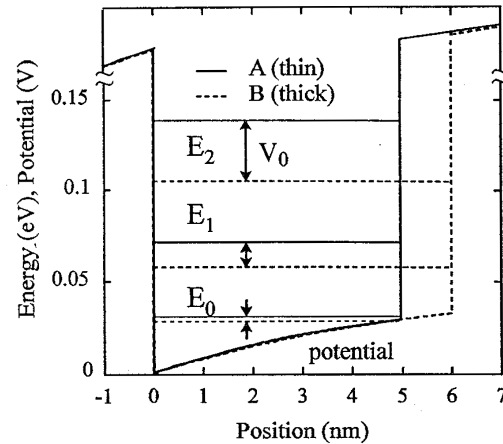

Fig. 5: Calculated band structure for two Si-layer thicknesses of 5 nm and 6 nm.

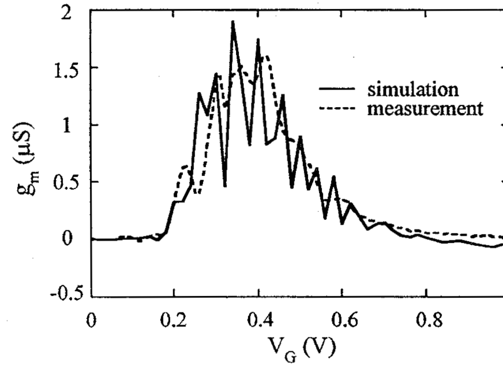

Fig. 6: Comparison of measured and simulated g_m values as a function of V_G with the barrier width $d = 30$ nm. Oscillation Amplitude and frequency are too big and too high.

3. Results

Figure 5 compares calculated energy levels for two different Si-layer thicknesses. It is obvious that the thinner Si-layer causes the higher barrier height. The barrier height difference is larger for higher energy level. Figure 6 shows calculated total g_m in comparison with measurements as a function of V_G at $V_D = 5$ mV. For the simulation two energy states (ground state and first-excited state) are considered.

Two parameters determine the structure of g_m oscillations. One is the barrier height V_0, namely the difference in the Si-layer thickness, and the other is the barrier width d. For this calculation $\Delta t_{si} = 1$ nm and $d = 30$ nm are employed. An Atomic Force Microscopy picture shows that the mean value of the terrace height is about 0.5 nm. Though we exaggerate the height, 1 nm is still within the technological fluctuation. Calculated oscillations show too big amplitude. Additionally the oscilla-

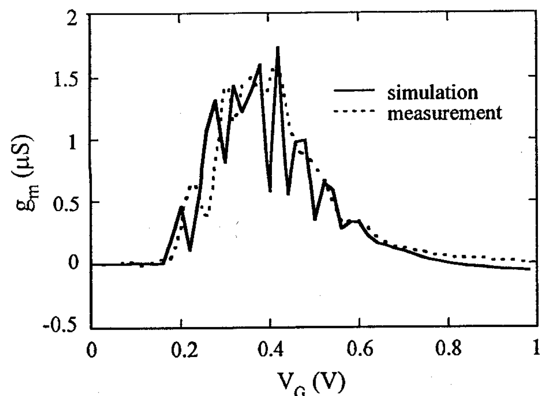

Fig. 7: Comparison of measured and simulated g_m values as a function of V_G. For the simulation $\Delta t_{si} = 1$ nm and $d = 20$ nm are choosen.

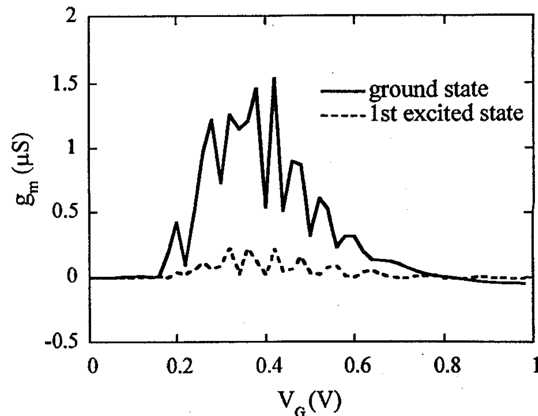

Fig. 8: Calculated g_m after its components, ground state and the first-excited state, as a function of the gate voltage V_G. By incleasing the V_G values, the contribution of the first-excited state on the g_m oscillation increases.

tion peaks are more than the measurement. Reducing the height of the terrace step by one half makes the energy quantization along the channel too small to observe the g_m oscillations. The oscillation frequency as a function of V_G is dependent on the barrier width d. By increasing d the frequency is increased and the amplitude is reduced at the same time. Figure 7 shows improved repreducibility of simulated g_m only by fitting the d value. The fitted d value is 20 nm.

From Fig. 5 it is expected that carriers at the higher energy state are more probably reflected by the barrier along the channel and causes dominant g_m oscillations. Figure 8 shows calculated g_m by its components. Here we took two states, ground state and first-excited state into consideration. For the whole V_G values, the contribution of the ground state is dominant. Especially for small V_G values carriers occupy only on the ground state. Relative small contribution of the first-excited state is due to small amount of carriers on the first-excited state in comparison with that of the ground state. The ratio of carrier density on the ground state to that on the first-excited state is roughly 9 : 1. However, above the threshold voltage, 0.2 V in this case, that of the first-excited state becomes feasible. At the end, for large V_G values only the first-excited state is responsible for the g_m oscillations. Unfortunately the g_m values themselves are too small to observe the contribution.

4. Conclusions

We have proposed a model describing the g_m oscillation of SOI-MOSFETs at low temperature. A consistent simulator including the model is developed here. The simulator is demonstrated to reproduce the measured g_m oscillations well. It is shown that carriers on the ground state are mainly responsible for the oscillation for low V_G values. However, the first-excited state becomes important for large V_G values.

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