Investigation to Suppress Hot Carrier Effect in Pocket–Implanted nMOSFET by Full Band Monte Carlo Simulation

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1 Introduction

Pocket (halo) implant processes are widely considered to be indispensable for deep submicron MOSFETs to suppress short channel effects such as roll-off of threshold voltage $V_{\rm th}$. It has been experimentally shown that a pocket device has a larger impact ionization (II) rate than a conventional device [1]. Bude *et al.* have also reported that halo (pocket) implant process enhances hot carrier (HC) injection into a gate electrode that can be utilized for programming stacked-gate memory cell transistor at the expense of device degradation [2]. This enhancement of HC injection has been mainly explained by impact ionization feedback (IIFB) mechanism [3]. However, to our knowledge no systematic study to optimize pocket implanted single gate MOSFETs with suppressed $V_{\rm th}$ roll-off and less HC generation/injection without performance deterioration has been reported.

In this paper, we will clarify two dimensional (2D) HC properties of the pocket implanted MOSFETs by full band Monte Carlo (MC) device simulation and the reason why HC generation can be suppressed with better $V_{\rm th}$ roll-off without deterioration of driving capability in some cases. We will also confirm it by measurements of gate and substrate currents I_g, $I_{\rm sub}$ and device lifetime τ of sub-quarter micron nMOSFETs.

2 Simulation

At first, steady state HC distributions for the following 0.18 μm gate length MOSFETs were investigated: (1) nMOSFET without pocket implantation *CON*-a, (2) nMOSFET with 30° tilted and thin pocket implantation *POC*-a, and (3) nMOSFET with non-tilted and thick pocket implantation *POC-b*, as shown in Tab. I and Fig. 1(a). The device structures were obtained by TSUPREM-4 using the same process flow as that of an experiment and calibrated to give the same drain current at a DAHC stress condition for all devices. The simulations were performed by our full band MC device simulator FALCON [4, 5] for 13 ps with a 0.1 fs time step at $V_g = 1.7$ V and $V_d = 3$ V, which is corresponding to the DAHC stress condition.

The calculated 2D distribution of the electron II generation rate is shown in Fig. 1(b). The electron II generation is found at the channel region as well as at the drain region. Fluxes of electrons that hit the silicon/gate-oxide boundary are shown in Fig. 2(a). Some hot electrons (HEs) at the channel region have more energy than the potential difference between the channel and the source region. Moreover, HEs of higher energy than $qV_d = 3.0$ eV are found in the drain region, which corresponds to a high energy tail up to 4 eV of the electron energy distribution functions shown in Fig. 2(b). These HC properties are explained by a mechanism called II feedback (IIFB) [3]. That is, a secondary hole generated by electron II at the drain region causes secondary hole II at the depletion region. The secondary II generates a very hot electron which gains energy from the built-in potential in addition to the supply voltage. Figure 3 shows electron and hole II generation rates and hole current vectors, clearly visualizing the IIFB process for the first time.

Compared to the conventional device (*CON*-a), as shown in Fig. 1(b), more II generation is found at the drain region in pocket devices (*POC*-a,*b*) because of the steeper well-drain *pn*-junction that causes higher electric field as indicated in the potential distribution of Fig. 1(c). However, we see in Fig. 2 less HEs in *POC-a* than in *CON*-a.

In order to clarify this reason the following one dimensional simulations were performed. First, one-dimensional potential distribution of each condition was extracted from two-dimensional potential distribution in Fig. 1(c) by the hole current trajectory from the maximum electron II position via hole II position to well region. Next, the steady state HC distributions were non-selfconsistently calculated with the potential distributions. Figure 4(a) shows the extracted potential as well as the II generation rate between the maximum electron II and hole II positions along the hole current tra-

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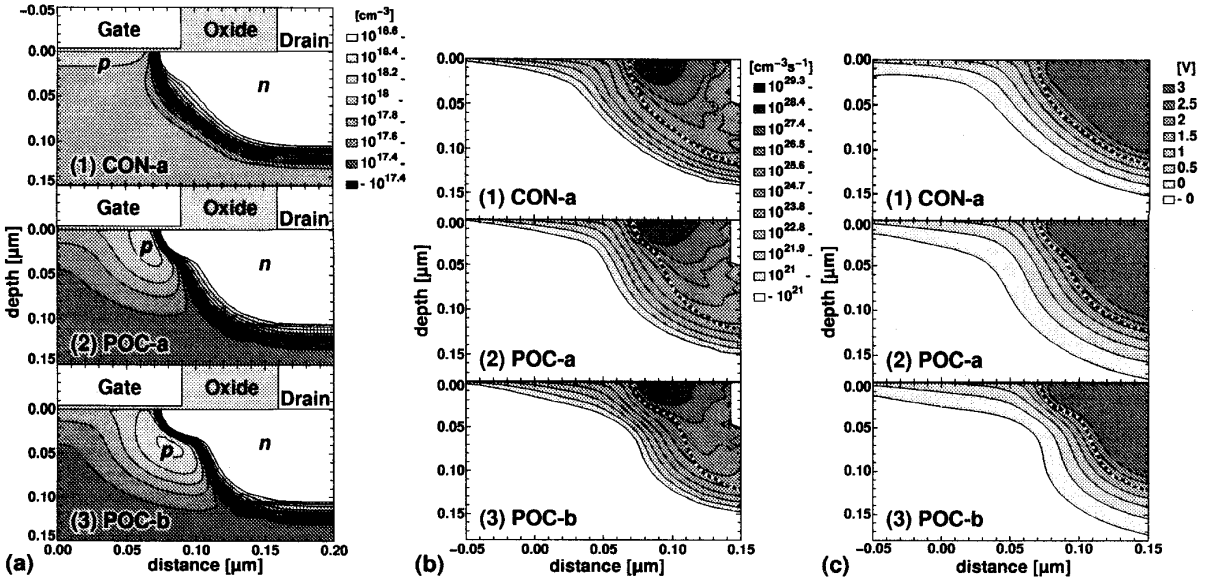

Figure 1: (a) Device structure for simulation, (b) calculated electron impact ionization generation rate, and (c) calculated potential distribution of three 0.18 μm nMOSFETs at $V_g = 1.7$ V, $V_d = 3$ V. The origin is at gate center and silicon/gate-oxide boundary. Dotted lines denote pn-junction.

jectory. In Fig. 4(b), distributions of HEs generated by the secondary hole II are shown. Though lower electric field at the well-drain junction in *CON-a* than in *POC-a* suppresses the peak of the hole II, the II occur in wider region. The II generates more HEs in *CON-a* than in *POC-a* as shown in Fig. 4(b). It is because *CON-a* has a wider region of a high electric field enough to gain energy for the hole II in contrast to *POC-a* with a wide depletion region of a low electric field due to thin $V_{\rm th}$ control implant. Therefore, angled and thin pocket implantation and thin $V_{\rm th}$ control implantation is effective to suppress HC generation of pocket devices.

3 Measurement

In order to confirm the simulation results, impact ionization rate $I_{\rm sub}/I_d$, $I_g/I_{\rm sub}$ ratios, and device lifetime τ of four kinds of nMOSFETs fabricated by our sub-quarter micron CMOS technology [6] were measured. The nMOSFET parameters are shown in Tab. II. Note that I_{ds} shows nearly the same for all the devices and that among the pocket ones there is no difference of $V_{\rm th}$ roll-off that is by far better than the conventional one. Figure 5 shows (a) measured $I_{\rm sub}/I_d$ ratios to estimate the primary electron II and (b) measured $I_g/I_{\rm sub}$ ratios to estimate the secondary hole II. Figure 6 shows device lifetime τ evaluated by 10 % degradation of S/D-reversed I_{ds}, where the stress bias condition for V_g is chosen to give $I_{\rm sub\,max}$ at each V_d in $V_{\rm sub} = 0, -2$ V cases.

As expected, even among the devices with the same $V_{\rm th}$ the thicker pocket implant induces more primary II as shown in Fig. 5(a) due to higher electric field at the well-drain junction and *CON-1* is the smallest in $I_{\rm sub}/I_d$ ratios. Moreover, Figs. 5(b) and 6 show the nMOSFET with more angled and thinner pocket implantation has less $I_g/I_{\rm sub}$ and longer τ. The most angled one *POC-1* has even less $I_g/I_{\rm sub}$ than *CON-1*. These results confirm our simulation results comparing *POC-a* and *CON-a*. However, the fact that *CON-1* has slightly longer τ in spite of more $I_g/I_{\rm sub}$ than *POC-1* indicates that τ does not completely depend on the amount and/or energy of HCs which are injected into the gate electrode.

4 Conclusion

We have clarified two dimensional HC properties of pocket implanted nMOSFETs by full band Monte Carlo device simulation, and we have shown that the HC generation can be suppressed keeping better $V_{\rm th}$ roll-off without deterioration of driving capability by properly choosing the pocket implant tilt angle. We have also confirmed it by measurements of gate and substrate currents and device lifetime of sub-quarter micron nMOSFETs.

References

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Table I: Parameters of simulated nMOSFET with $L_{\rm poly}$ = 0.18 μm.

name	pocket *II* tilt °	pocket *II* dose cm^{-2}	$V_{\rm th}$ control *II* dose cm^{-2}
CON-a	—	—	1.7×10^{13}
POC-a	30	3.4×10^{13}	5.8×10^{12}
POC-b	0	6.4×10^{13}	5.8×10^{12}

Table II: Parameters of measured nMOSFET with $L_{\rm poly}$ = 0.18 μm. $\Delta V_{\rm th}$ is difference of $V_{\rm th}$ between $L_{\rm poly}$ = 0.18 μm and 0.16 μm.

name	pocket *II* tilt °	pocket *II* dose cm^{-2}	$V_{\rm th}$ control *II* dose cm^{-2}	$V_{\rm th}$ (V_{dd} = 1.8 V) V	I_{ds} (V_{dd} = 1.8 V) μA/μm	$\Delta V_{\rm th}$ V
CON-1	—	—	1.6×10^{13}	0.39	521	0.104
POC-1	30	2.0×10^{13}	8.0×10^{12}	0.38	514	0.026
POC-2	15	3.2×10^{13}	8.0×10^{12}	0.37	516	0.024
POC-3	7	4.0×10^{13}	8.0×10^{12}	0.38	508	0.024

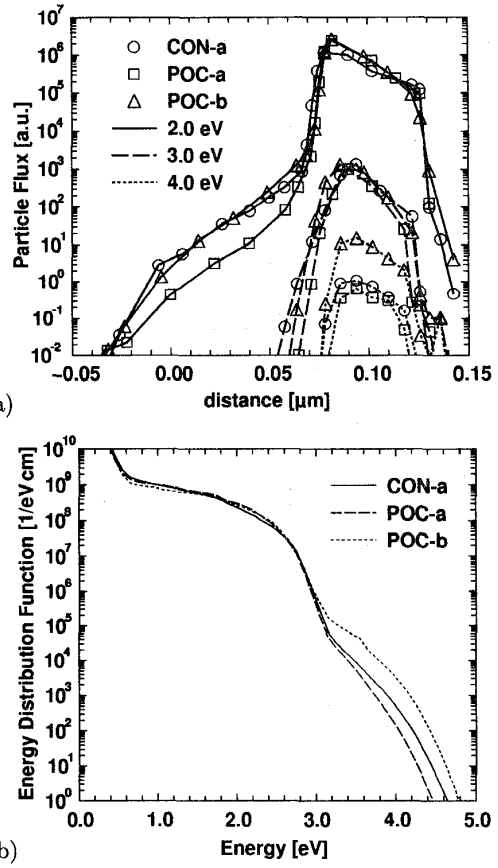


Figure 2: (a) Flux of electrons which hit the silicon/gate-oxide boundary and (b) energy distribution function of electrons in the whole silicon region at V_g = 1.7 V, V_d = 3 V.

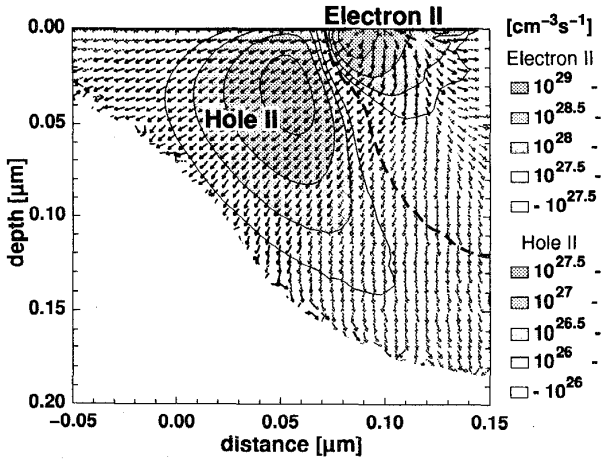
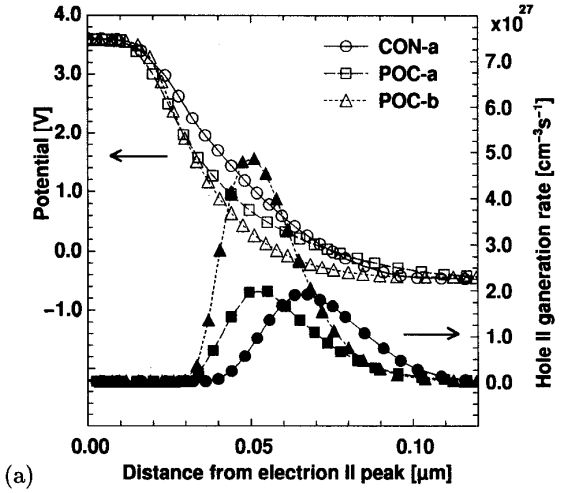


Figure 3: Distribution of electron and hole impact ionization generation rates (contour) and hole current (allows) of *POC-a* at V_g = 1.7 V, V_d = 3 V. Dashed line denotes the *pn*-junction.



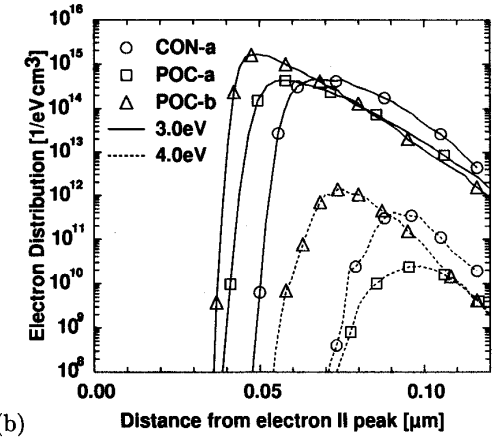
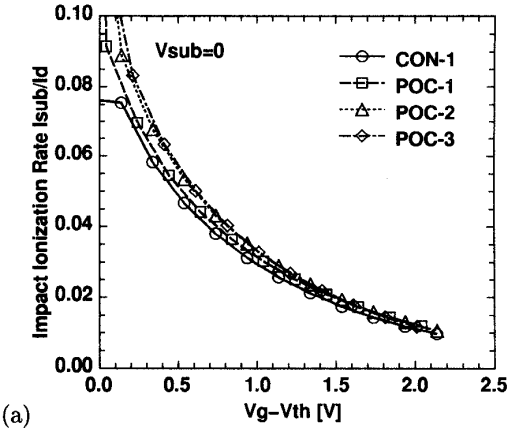


Figure 4: (a) Extracted potential and calculated hole impact ionization (II) generation rate and (b) calculated distribution of electrons with energy of 3.0, 4.0 eV by 1D simulation from electron II peak position via hole II peak position to well region along hole current trajectory.



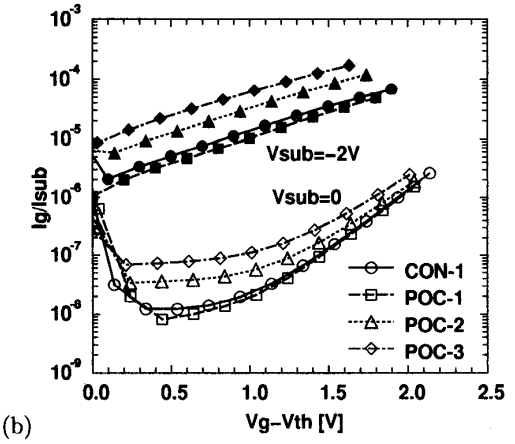


Figure 5: Measured (a) $I_{\rm sub}/I_d$ ratios at $V_d = 3$ V, $V_{\rm sub} = 0$ V and (b) $I_g/I_{\rm sub}$ ratios at $V_d = 3$ V, $V_{\rm sub} = 0, -2$ V as a function of $V_g - V_{\rm th}$ for four kinds of nMOSFET in Tab. II.

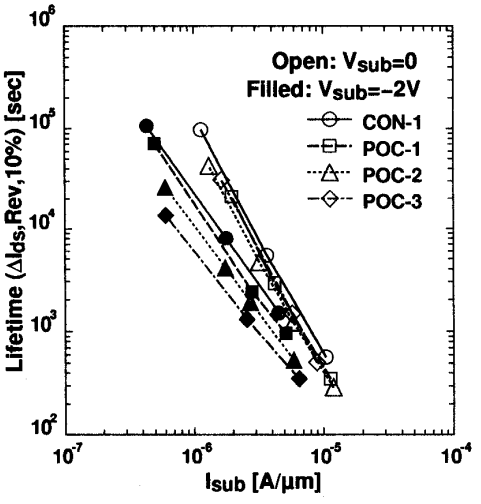


Figure 6: Measured device lifetime as a function of $I_{\rm sub}$. The lifetime is evaluated by 10 % degradation of S/D-reversed I_{ds}. The stress bias condition for V_g is chosen to give $I_{\rm sub\,max}$ at each V_d in $V_{\rm sub} = 0, -2$ V cases.