Monte Carlo Investigation of Optimal Device Architectures for SiGe FETs

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Strained silicon channel FETs grown on virtual SiGe substrates show clear potential for RF applications, in a material system compatible with silicon VLSI. However, the optimisation of practical RF devices requires some care. 0.1–0.12μm gate length designs are investigated using Monte Carlo techniques. Although structures based on III-V experience show f_T values of up to 94 GHz, more realistic designs are shown to be limited by parallel conduction and ill constrained effective channel lengths. Aggressively scaled SiGe devices, following state–of–the–art CMOS technologies, show f_T values of up to 80 GHz.

1. Introduction

Both theoretical and experimental studies show that low field mobility and velocity overshoot are enhanced in Si layers grown pseudomorphically on relaxed SiGe substrates. The induced strain breaks the six fold degeneracy of the Si Δ valleys, resulting in an improved band offset for the two conduction band valleys whose transverse mass is in the plane of the heterojunction. This increases the in–plane mobility and reduces the intervalley scattering in the Si layer [1,2].

Modulation doped field effect transistors (MODFETs) exploiting such strained Si channels have been demonstrated and show clear potential for RF applications [3,4]. Although measured mobilities do not approach those reported in optimal III-V devices, mobilities are found to be higher than those of bulk silicon, the channel does isolate conduction electrons from interface roughness scattering, and devices are compatible with conventional Si technology. This makes SiGe devices attractive for Si MMIC design and microwave signal processing applications integrated with conventional Si components.

However, the confinement obtained in a strained channel grown on a 30% $Si_{1-x}Ge_x$ virtual substrate is only of the order of 180 meV, and many of the techniques used in the design of III-V devices (such as δ-doping and recessed gate technology) cannot be assumed to be either available or appropriate to Si fabrication. Thus the design of practical RF devices requires care in optimisation. In this paper, a number of 0.10 – 0.12 μm gate length designs are investigated using Monte Carlo techniques. Insight is gained into the potential of SiGe devices, optimal structures are suggested, and performance is compared to the latest silicon MOSFETs.

2. Device Structures and Analysis Tools

Idealised Devices

Figure 1(a) shows a strained silicon channel MODFET based on the vertical layer structure of a state–of–the–art InGaAs pseudomorphic HEMT, with a T–shaped recessed gate and heavily doped cap layers. The gate length is 120 nm with gate to channel separation of 20 nm. A 5×10^{12} cm^{-3} δ-doped layer is placed 2.5 nm above the channel. This device is based on present III-V design experience [5] primarily conjecturing improvements in growth technology and low temperature processing to allow formation of a well defined As δ-doped supply layer. Thus the design will indicate the performance potential of SiGe MODFETs. To simplify modelling, a uniform SiGe substrate is assumed, rather than a 'virtual' substrate with graded Ge concentration. The nominally Si etch stop region of the device is also considered as (undoped) SiGe. Simple 1D Poisson–Schrödinger calculations indicate that if a strained Si etch stop region is included, it will exhibit negligible parallel conduction at d.c. bias points up to $V_G = 0$ V.

It is predicted [6] that SiGe MOSFETs will exhibit greater RF performance than equivalent MODFETs. Figure 1(b) shows such a device, with channel length of 120 nm. Both the MODFET and MOSFET have electro-statically equivalent gate to channel separation.

Practical Devices

As noted above, present fabrication technology precludes the use of δ-doping due to high dopant diffusion rates. In its absence, a structure such as that of figure 1(c) is appropriate. To achieve high transconductance the gate–channel separation should be as small as possible. To avoid the early onset of parallel conduction at the SiO_2 interface the spacer and supply layers should be as thin as possible and the supply layer doped highly. With present technology, the

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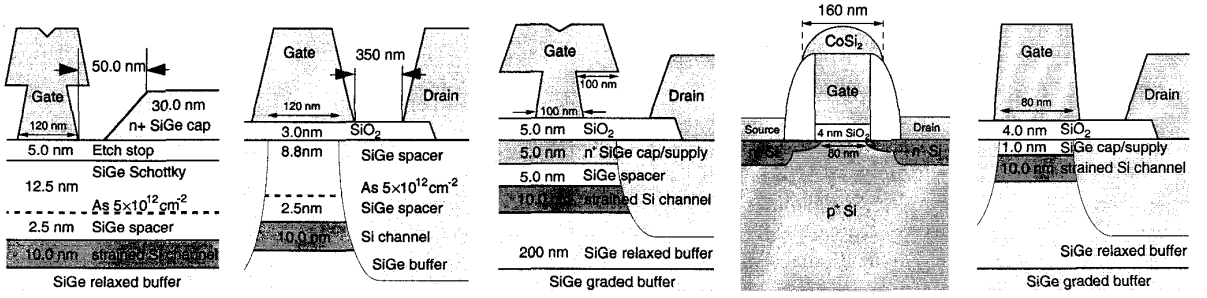

Fig.1 Device structures of various Si and SiGe n-channel FETs studied in this work: (a,b) SiGe modulation doped devices with equivalent gate-to-channel separation, (c) fabricable SiGe MOSFET, (d,e) state of the art Si MOSFET and equivalently scaled SiGe MOSFET.

limitations on this structure are set by the need to avoid dopants diffusing through the SiGe spacer into the channel under the influence of realistic thermal fabrication budgets, and the ability to grow thin oxide layers (itself a function of the quality of the sacrificial Si layer atop the highly doped SiGe supply layer) [7]. The gate–channel separation will ultimately be limited by the remote effects of SiO_2 interface roughness on channel mobility as the spacer is reduced, and the need to control the gate tunnelling current through ultra–thin gate oxides.

Figure 1(c) describes an RF self aligned T-gate MOSFET within the bounds of present fabrication technology.

Future Devices

An alternate method for achieving optimum performance is to modify an aggressive silicon MOSFET, such as that of figure 1(d), a Co salicided T-gate style RF device with measured f_T of 65 GHz [8]. Here, the T–gate structure is formed as part of a raised gate/source/drain CMOS process, rather than using multi–level resist processing. A SiGe device based on this technology and simplified for ease of simulation is shown in figure 1(e) with a channel–oxide separation of 1 nm and a 4 nm oxide. In simulating both the Si and SiGe MOSFET, the gate, oxide and contact geometries of figure 1(e) are used to allow better device comparison.

Monte Carlo Analysis

All of the devices considered are modelled using the Monte Carlo module of the finite element simulator H2F [9]. We follow Yamada's [1] treatment of the effect of strain on the Si channel bandstructure, with conduction band splitting of $\Delta E_c = 0.67x$ (eV) and band gap energy $E_g = 1.11 - 0.74x$ (eV). The six phonon scattering model of Jacoboni [10] is implemented, and ionised impurity scattering is calculated from the Brooks-Herring model [11]. Bulk velocity–field characteristics obtained from the model are in agreement with experimental unstrained Si data at 77 K and 300 K and previous results for strained Si [1,2]. At present, interface roughness scattering is not included in these device models.

RF analysis

To obtain small signal equivalent circuit data and RF figures of merit, Monte Carlo simulations follow 5×10^4 superparticles within these devices on application of a step input voltage change $\Delta V_G = 0.2$ V or $\Delta V_D = 0.3$ V. The transient response is measured for 5.0 ps, with the Ramo–Shockley theorem [12] being used to efficiently calculate terminal currents, reducing the effects of statistical noise over purely 'superparticle counting' methods. It is found that structure and doping dependant THz oscillations in device drain currents (possibly due to plasma oscillations in the channel or heavily doped regions) may mask the detailed form of the transients. Therefore multiple traces are averaged to define the response.

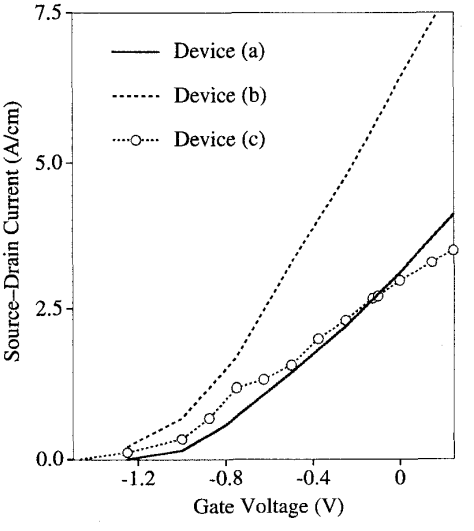

Fig.2 Transfer characteristics of devices (a) - (c) from Monte Carlo simulation of 50 000 particles for 6.0ps after 2.0ps settling time. $V_D = 1.5$V. Device width of 100μm assumed.

Complex y-parameters are derived by Fourier transforming the terminal currents, and used to extract the

small signal equivalent circuit. The cut-off frequency of the simulated device, f_T, is extracted by solving $\log [G_C(\log f)] = 0$ where $G_C = dI_d/dI_g$ is the current gain expressed as a function of y-parameters. In order to extract the maximum frequency of oscillation of the simulated device, f_{max}, the y-parameters are transformed into the s-parameters. f_{max} is then extracted by solving $\log [MAG(\log f)] = 0$ where MAG is the maximum available gain. Finally, the small signal equivalent circuit is augmented by the addition of external gate and contact resistances, and thus the effect of contact and gate resistance on the 'real' device operation is estimated.

3. Results and Discussion

Figure 2 and Table I show the transfer characteristics and intrinsic small signal equivalent circuit parameters obtained from our Monte Carlo simulations of devices 1(a,b,c). Figures of merit resulting from the inclusion of realistic contact/access resistances are shown in Table II. Figure 3 shows the channel drift velocities (with 0 signifying the rhs gate edge) found when these devices are biased at $V_G = -0.2$ V. At this bias both of the δ-doped devices achieve maximum transconductance within the limit that parallel conduction should be less than 10% of total drain current. All of the modelled devices show significant velocity overshoot along the strained silicon channel. As predicted, the modulation doped MOSFET outperforms the equivalent MODFET, improving transconductance by over 50%, and suggesting that an f_T of 94 GHz is possible. The performance of the MOSFET results from better 'confinement' of the active region by the self aligned source–drain implants, resulting in reduced effective channel length. This is shown clearly in figure 3.

In general, inclusion of realistic gate, source and drain access resistances reduce the maximum frequency of oscillation, f_{max}, by at least twice as much as the threshold frequency, f_T. The structure of the MOSFET device gives larger small signal equivalent circuit capacitances. Thus the effects of realistic access resistances are more pronounced in the MOSFET, and its advantages, in practical devices, may be lost.

Table I Small signal equivalent circuit parameters for devices (a) - (c) calculated from $\Delta V_D = 0.3$V, $\Delta V_G = 0.2$V step functions and simulated 5ps transient response. Device width of 100μm assumed.

Parameter	MODFET device (a)	MOSFET device (b)	MOSFET device (c)
C_{gs} (fF)	59.3	101	89.1
C_{gd} (fF)	22.3	27.0	30.5
C_{ds} (fF)	12.4	21.3	25.3
g_{mo} (mS)	38.8	60.6	25.8
g_{ds} (mS)	8.5±1	8.7	3.8
R_i (Ω)	5.9	4.5	6.5
τ (ps)	0.15	0.32	0.31

Table II RF figures of merit for devices (a) - (e). Biased about maximum transconductance and calculated from simulated 5ps transient response to $\Delta V_D = 0.3$V, $\Delta V_G = 0.2$V. Device (c) biased at max. transconductance without/with parallel conduction.

Figures of Merit	devices (a)	(b)	(c)	(d)	(e)
	with negligible contact resistance				
f_T (GHz)	80	94	45/36	90	80
f_{max} (GHz)	171	187	154/96	380	250
	gate, source & drain resistance 1Ω				
f_T (GHz)	78	88	45/36	85	70
f_{max} (GHz)	135	127	122/78	200	160
	gate, source & drain resistance 5Ω				
f_T (GHz)	70	71	43/34	80	60
f_{max} (GHz)	82	66	77/49	100	60

The performance of the realistic device design, 1(c), proves to be disappointing compared to that of the δ-doped devices. Firstly, the onset of parallel conduction can be clearly seen in the structure of its transfer curve. Below -0.25 V the channel dominates and a g_{mo} of approximately 400 mS/mm is obtained, but as parallel conduction increases g_{mo} falls to 250 mS/mm (Table 1 is calculated at V_G=0 V). The onset of parallel conduction will improve as fabrication advances allow reduced spacer layer thickness. However from Table II it can be seen that the performance of device 1(c) is disappointing even when operating without parallel conduction.

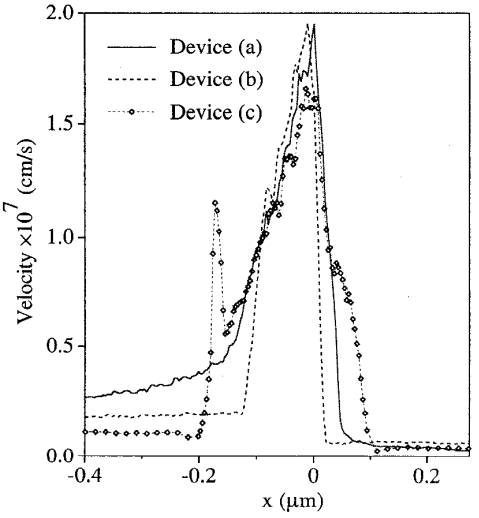

Fig.3 Electron drift velocities in the strained silicon channel of devices (a) - (c). $V_D = 1.5$V, $V_G = -0.2$V.

Figure 3 shows that whilst devices 1(a,b) have an effective channel length of approximately 150 nm to 200 nm, in device 1(c) it extends over approximately 300 nm,

markedly reducing performance. Effective channel lengths in this FET will require control - either by aggressively scaling the gate oxide, or by angling source and drain implants under the wings of the T-gate.

Modelled transfer characteristics for devices 1(d,e) are shown in figure 4, with figures of merit listed in Table II. Due to the structure of these devices, with their smaller ratio of active region to heavily doped implants, the transient Monte Carlo results include more statistical noise for equivalent processing time than devices 1(a,b,c). This is reflected in the number of significant digits in their figures of merit.

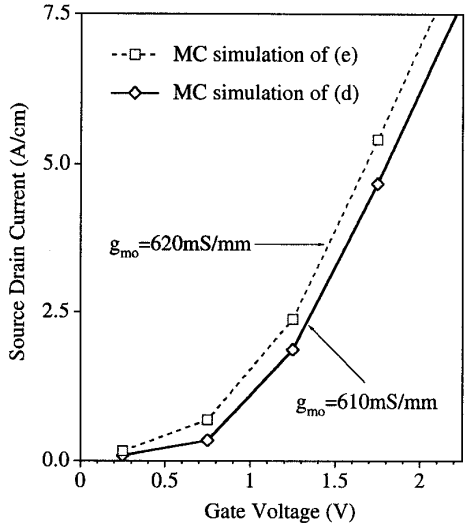

Fig.4 Transfer characteristics of devices (d)-(e) from Monte Carlo simulation of 50 000 particles for 6.0ps. V_D = 1.5V.

Although the Si FET does not benefit from the increased mobility of the strained Si channel in the SiGe device, it does have a smaller gate–channel separation, and critically, interface roughness scattering is ignored. With realistic access resistance this modelled Si FET has threshold frequency 20 GHz higher than that of the experimentally measured device. Both simulated devices have comparable transconductances and threshold frequencies.

4. Conclusions

The performance of various strained Si channel MODFETs and MOSFETs has been investigated using transient Monte Carlo simulation techniques. Structures based on III-V device experience show f_T values of up to 94 GHz. Although simulation of practical devices shows them to be severely limited by parallel conduction and ill constrained effective channel lengths, techniques for improving their performance are noted. Practical, aggressively scaled SiGe devices in the style of state–of–the–art CMOS technology are modelled and show f_T values of up to 80 GHz, although equivalent Si FET performance is comparable if interface roughness scattering is ignored.

References

1. T. Yamada, J. Zhou, H. Miyata and D.K. Ferry: IEEE Trans. Elec. Devices, **41** (1994) 1514.
2. J.B. Roldán, F. Gámiz, J.A. López-Villanueva and J.E. Carceller: J.Appl.Phys. **80** (1996) 5121.
3. J. Welser, J. L. Hoyt and J. F. Gibbons: IEEE Electron Device Letters **14** (1993) 348.
4. K. Ismail, S. Rishton, J. Chu, K. Chan and B. Meyerson: IEEE Electron Device Letters **14** (1993) 348.
5. A.Asenov, S. Babiker, N. Cameron, S. Murad, M. Holland and S. P. Beaumont, *NATO ASI Series, Devices Based on Low Dimensional Semiconductor Structures*, Kluwer Academic Series (1996).
6. A. O'Neill, D. A. Antoniadis: IEEE Trans. Electron Devices **44** (1997) 80.
7. A. Churchill: *private communication.*
8. T. Ohguro, H. Naruse, H. Sugaya, S. Nakamura, E. Morifuji, H. Kimijima, T. Yoshitomi, T. Morimoto, H. S. Momose, Y. Katsumata and H. Iwai, *IEEE Symposium on VLSI Technology* (1998) 163.
9. S. Babiker, A. Asenov, N. Cameron, S. P. Beaumont and J. R. Barker: IEEE Trans. Electron Devices **45** (1998) 1644.
10. C. Jacoboni and P. Lugli, *The Monte Carlo Method for Semiconductor Device Simulation*, (Springer–Verlag, Wein, 1989)
11. H. Brooks: Physical Review **83** (1951) 879.
12. H. Kim, H. Min, T. Tang and Y. Park: Solid State Electronics **34** (1992) 1251.