DRAM Bit-line Coupling Noise Analysis and Simulation of Process Sensitivity for COB Scheme

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The bit-line coupling capacitance and its process sensitivity of $8F^2$ cell in COB scheme are critical issues for future advanced DRAM. In this paper, these issues and design curves of bit-line coupling capacitance of $8F^2$ cell in COB scheme are investigated by 3D simulation and analytical model.

1. Introduction

The bit-line inter-coupling noise [1-5] in DRAM is a critical challenge for future multi-gigabit DRAM. The cell capacitor of stack DRAM is typically fabricated before or after the formation of bit-line and is referred to as Capacitor-Under-Bitline (CUB) or Capacitor-Over-Bitline (COB) schemes respectively. The COB scheme replaced CUB scheme since 16Mbit DRAM generations due to advantages of larger possible foot-print of capacitors in COB scheme. Although the bit-line coupling in COB scheme is smaller [6] than CUB scheme due to the blocking of capacitor node in-between bit-lines; however, their sensitivity to process parameters has not been systematically analyzed.

In this paper, the process sensitivity and design curves of bit-line coupling capacitance of $8F^2$ cell in COB scheme are investigated by 3D simulation. A lumped capacitor-resistor model for bit-line coupling noise in folded bit-line DRAM array is also presented.

2. Analysis of Intercoupling Capacitance

A sketch of $8F^2$ cell [8,9] layout and cross-section with crown capacitor in COB scheme is shown in Fig. 1. The plate layer is on the inside (and/or outside) of the crown capacitor. The bit-line is connected to the substrate through poly plugs. The crown capacitor is connected to the node junction also through poly plugs. The bit-line and node are separated by a spacer of nitride or oxide. The dielectric between conductors is assumed to be SiO_2 (ε_r~3.9).

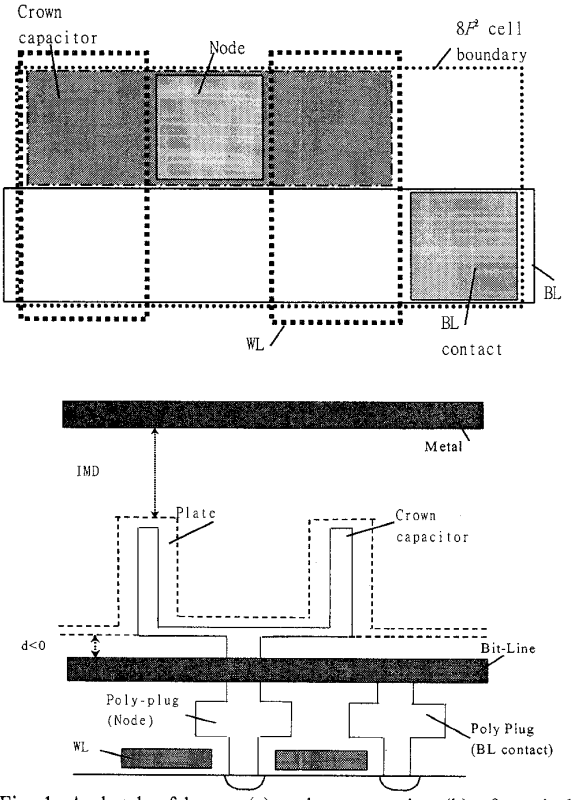

Fig. 1: A sketch of layout (a) and cross-section (b) of typical $8F^2$ cell structure with crown capacitor in COB schemes (not to scale).

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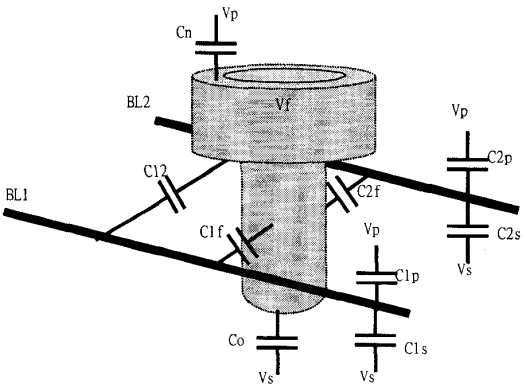


Fig. 2. Notations of capacitance components of two bit-lines and one node capacitor in COB scheme of DRAM.

The corresponding capacitor components and notations are sketched in Fig. 2. The node poly plug is floating (entirely surrounded by insulting materials) and connected to C_n (i.e. the cell capacitance ~30fF) and C_o (i.e. the node-junction and node-wordline capacitances). C_{12} is the coupling capacitance for the bit-line section facing each other directly. C_{1f} and C_{2f} are the capacitances from bit-line to node electrode, which is inversely proportional to the spacer thickness. C_{1p} (C_{2p}) is the bitline BL1 (BL2) to plate capacitance. C_{1s} and C_{2s} are the bit-line to junction capacitances. The plate bias (V_p) is typically $V_{cc}/2$. The substrtate bias (V_s) is typically -1v at 0.25um DRAM technology. The net charge and potentials on the cell capacitor, bit-lines (BL1 and BL2) are denoted as Q_f, Q_1, Q_2 and V_f, V_1, and V_2 respectively. The charge conservation law enforced on the cell capacitor node and bit-lines is,

$$C_{1f}(V_f-V_1)+C_{2f}(V_f-V_2)+C_n(V_f-V_p)+C_o(V_f-V_s)=Q_f \quad (1)$$

$$C_{1f}(V_1-V_f)+C_{1p}(V_1-V_p)+C_{1s}(V_1-V_s)+C_{12}(V_1-V_2)=Q_1 \quad (2)$$

$$C_{2f}(V_2-V_f)+C_{2p}(V_2-V_p)+C_{2s}(V_2-V_s)+C_{12}(V_2-V_1)=Q_2 \quad (3)$$

Mathmatically, the inter-bitline coupling capacitance C_{blbl} is easily represented as,

$$\frac{dQ}{dV_2}=(\partial Q_1/\partial V_2)+(\partial Q_1/\partial V_f)(\partial V_f/\partial V_2)\equiv -C_{blb}$$

where the 1st term corresponds to the direct coupling through C_{12}, and the 2nd term corresponds to the indirect coupling through C_{2f} to node and C_{1f}. From (1) and (2), the intercoupling capacitance C_{blbl} is easily derived,

$$C_{blbl} = C_{12} + \frac{C_{1f}C_{2f}}{C_{1f}+C_{2f}+C_n+C_o} \quad (4)$$

The total bit-line capacitance C_{bltot} in array can be similarly derived as,

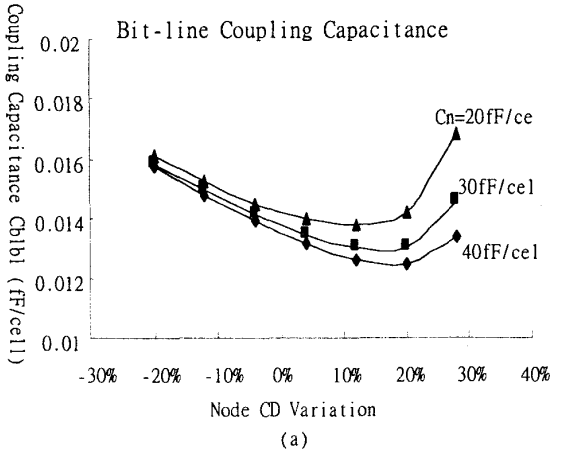
$$C_{bltot} = C_{1p} + C_{1s} + 2C_{blbl} + \frac{(C_{1f}+C_{2f})(C_n+C_o)}{C_{1f}+C_{2f}+C_n+C_o} \quad (5)$$

The process sensitivities of coupling capacitance can be understood from (4). The cell capacitance C_n can impact the shielding of bit-lines. Typically, the cell capacitance is designed to be large (~30fF/cell), i.e. $C_n >> C_{1f}$ or C_{2f}, therefore, $C_{blbl}=C_{12}$. However, if C_n is smaller (e.g. in defective bit), C_{blbl} can be significantly larger than C_{12} and further degrade the cell sensing process with more coupling noise. The node size and un-even spacer thickness can result in un-symmetrical C_{1f} and C_{2f}, and this in turn can result in larger C_{blbl} as predicted from (4). The variations of capacitance components due to process variations are simulated using 3D simulator as described below.

3. 3D-Simulation and Process Sensitivities

The bit-line coupling capacitance is simulated [10] using 3D capacitance solver Raphael RC3[11] with reflective boundary conditions. The typical cell capacitance is designed to be 30fF. The DRAM cell foot-print is $4Fx2F$ ($=8F^2$) based on DRAM technology with folded-bitline array architecture. The feature size F and transistors are calibrated based on typical 0.18um to 0.25um stack DRAM technology.

The 3D simulated bit-line coupling capacitance (C_{blbl}) and total bit-line capacitance (C_{bltot}) with respect to the node contact size is shown in Fig. 3 with cell capacitance C_n as a parameter. Interestingly, there is a minimum in each curve. This is due to a combined effect of node contact size to C_{1f} and C_{2f}, as well as C_{blbl}. The ratio of C_{blbl}/C_{bltot} which is a key parameter [12] to the bit-line coupling noise transients on bit-lines is shown in Fig. 3c. A 10% node contact size variation can result in ~20% variations of the ratio of C_{blbl}/C_{bltot}. Smaller cell capacitance C_n would result in larger ratio of C_{blbl}/C_{bltot}.



(a)

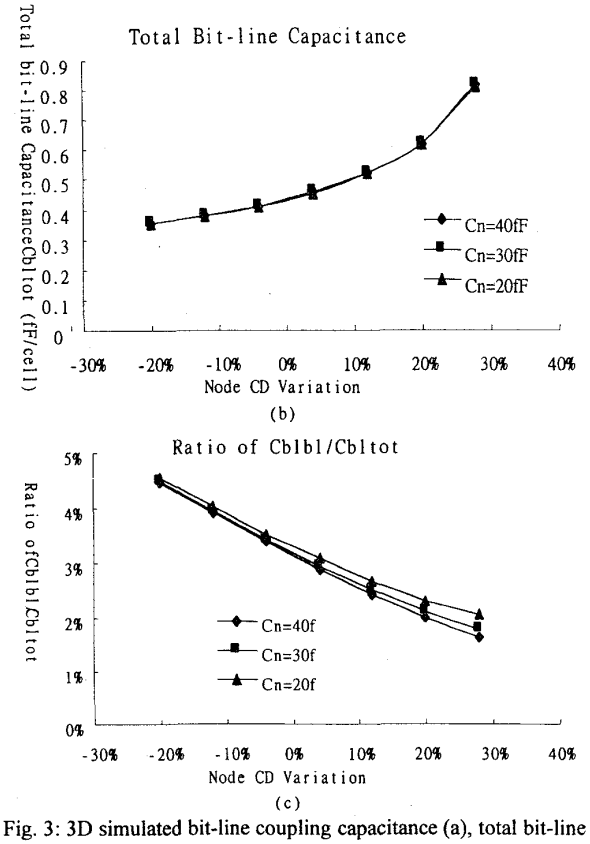
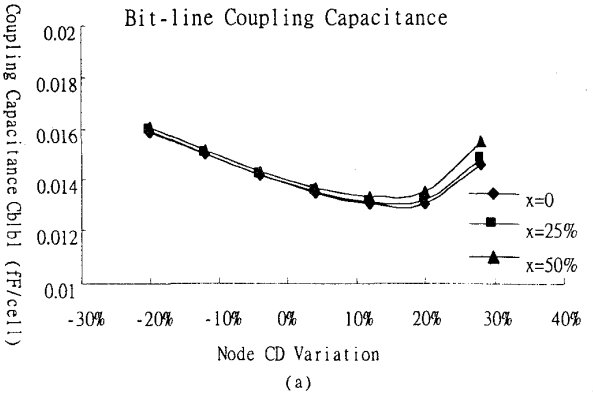


Fig. 3: 3D simulated bit-line coupling capacitance (a), total bit-line capacitance (b), and the ratio of C_{blbl}/C_{bltot} (c) with respect to node contact size and with C_n as a parameter.

Fig. 4 shows the effect of un-even spacer thickness along the two sides of bit-line edges. The degree of un-even spacer thickness is represented by the % deviation from its ideal value. A larger un-even spacer thickness results in larger C_{blbl} and C_{bltot} but less C_{blbl}/C_{bltot} (i.e. noise transients) as shown in Fig. 4c.



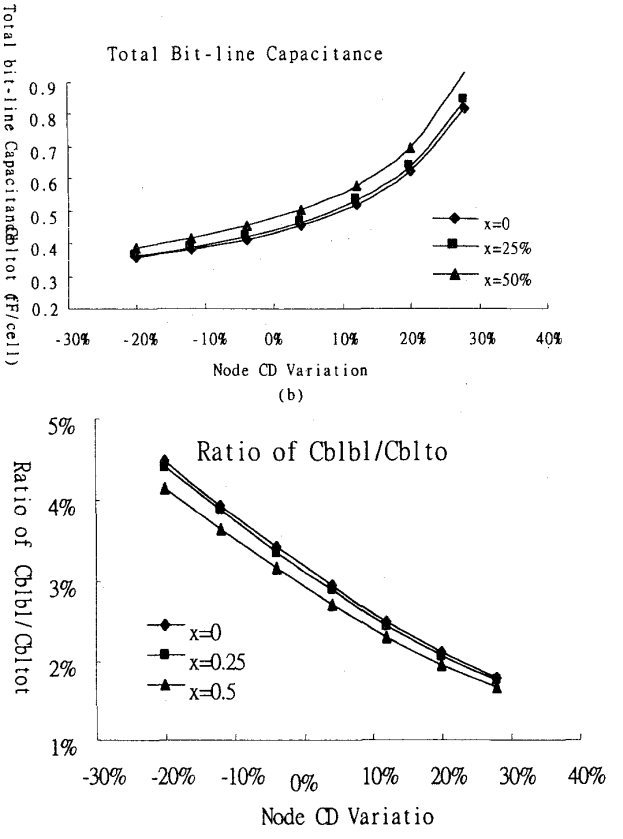


Fig. 4: 3D simulated bit-line coupling capacitance (a), total bit-line capacitance (b), and the ratio of C_{blbl}/C_{bltot} (c) with un-even spacer thickness x as a parameter.

4. Analysis of Inter-coupling Noise Transients

Noise transients on bit-lines may occur during sensing operation through capacitive coupling from adjacent bit-lines (e.g. adjacent bit-lines are driven to V_{cc} or V_{ss} by the sense amplifier). The noise transient from capacitive coupling from one adjacent bit-line can be modeled by lumped capacitor-resistor model [13] as shown in Fig. 5. The sense amplifier is modeled as an ideal unit-step voltage source V_{SA} with output capacitance C_{SA}. The coupling noise $V_n(t)$, (normalized to the step voltage V_{SA}) can be shown analytically [12] as,

$$V_n(t) = (1/2).\{\exp(-t/t_1) - \exp(-t/t_2)\} \quad (6)$$

Where $t_1=R(C+C_{SA})$ and $t_2=R(2C_{blbl}+C+C_{SA})$. R is the bit-line resistance, C is the bitline-to-ground capacitance (i.e. not including the coupling capacitance C_{blbl}). Notice that the bit-line junction capacitance is included into the capacitor C in the model. The maximum coupling noise (V_{max}) is easily derived by setting the time differential of $V_n(t)$ to zero. A calculated noise transient of a typical 0.18um $8F^2$ DRAM cell is shown in Fig. 6.

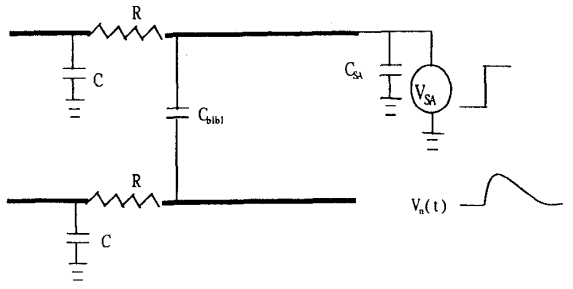


Fig. 5: A simple model using lumped capacitor-resistor components for estimating noise transient from adjacent bit-line.

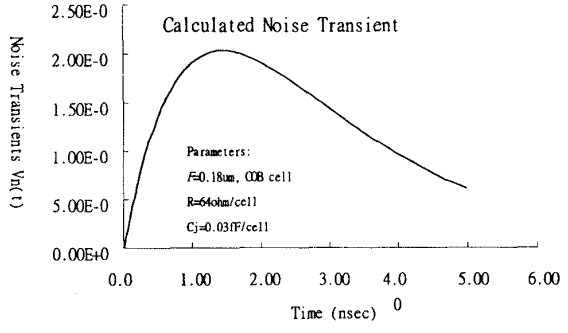


Fig. 6: A normalized noise transient of typical $8F^2$ DRAM cells with COB scheme.

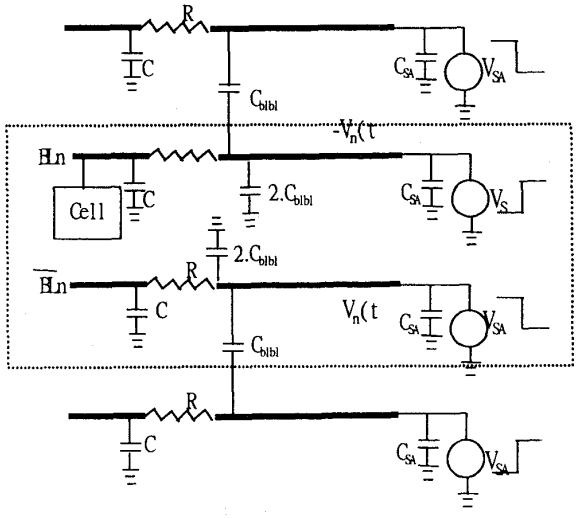


Fig. 7: A lumped capacitor-resistor model for bit-line coupling noise analysis in folded bit-line DRAM array. The polarity of sense amplifier voltage sources can result in worst case coupling noise to the bit-line pair under sensing.

The above simple model can be extended for estimating the bit-line noise transients in folded bit-line array, where bit-lines are paired with half-V_{cc} bias scheme and shared sense amplifier [5]. The worst case noise coupling occurs when the voltage transients coupled into the bit-line pair from adjacent bit-lines with opposite polarity to the signal from the cell being read as sketched in Fig. 7. With the worst case coupling noises, the effective differential signal seen by the sense amplifier of the (n^{th}) bit-line pair is (V_{sig} – $2.V_{max}.V_{cc}/2$), i.e. V_{sig} -V_{max}.Vcc. Notice that the intra-bitline coupling capacitance within the bit-line pair is molded as $2.C_{blbl}$ to ground due to the differential signal toward V_{cc} or V_{ss} (from $V_{cc}/2$) by the driving of sense amplifier. The signal V_{sig} from the selected DRAM cell is typically ~200mv. Thus, when V_{max} is large enough (~V_{sig}/V_{cc}), the sensing will be slow and even erroneous. Thus V_{max} must be smaller than V_{sig}/V_{cc}.

5. Conclusion

In summary, the bit-line coupling capacitance and its process sensitivity of $8F^2$ cell in COB scheme is a critical issue for future advanced DRAM. The 3D simulation and analysis demonstrate that the bit-line coupling capacitance of COB scheme is sensitive to process parameters, e.g. increasing C_{blbl} at smaller node capacitance, larger node contact size, and un-even spacer thickness.

The capacitance model with floating capacitors can be easily modified and applied to the noise transients in word-lines in DRAM array. Similar model can be useful for studying the noise transient effect on control lines and bit-lines in other memory arrays such as EEPROM, EPROM, ROM, or Flash memory.

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