Two- and three-dimensional simulations of anomalous current in small-dimension pn junctions integrated with an ultra-high density

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1. Introduction

As the integration scale of LSIs increases, device dimensions are being drastically miniaturized. When extremely small pn junctions are integrated at an ultra-high density, unexpectedly high-level leakage currents, larger than the normal level by a factor of 10^2 - 10^3, have been observed in the tail of the cumulative failure distribution for the retention times of DRAMs [1] (Fig. 1(a)). These currents frequently show a steep increase and high level saturation (Fig. 1(b)). During LSI fabrication, heavy implantations are used, which might induce defects or heavy-metal contamination. Assuming a locally generated deep-trap model [2], we analyze the anomalous currents shown in Fig. 1(b) through two- and three-dimensional device simulations.

2. Modeling

Based on the classical drift-diffusion (D-D) modeling, the current flowing through pn junctions is analyzed. The current continuity equations for electrons and holes are given as;

$$\nabla J_n = R, \quad (1)$$

$$\nabla J_p = -R. \quad (2)$$

The generation/recombination (g/r) rate, which indicates the contribution of deep-traps, for example, donor-type traps, is modeled as follows;

$$R_{DD} = \frac{np - n_1 p_1}{(n+n_1)/C_p + (p+p_1)/C_n} N_{DD}, \quad (3)$$

where n and p are the electron and hole densities, and C_n and C_p are the capture rates for electrons and holes. Parameters n_1 and p_1 are given by;

$$n_1 = n_i \times \exp((E_t - E_i)/k_B T), \quad (4)$$

$$p_1 = n_i \times \exp((E_i - E_t)/k_B T), \quad (5)$$

where E_t is the energy level of the trap center. The g/r rate for the acceptor-type deep-traps, R_{DA}, is also modeled using the same functional formula. The above modeling has been frequently utilized in compound semiconductor device analysis [3], [4]. The total g/r rate R is given by ($R_{DD} + R_{DA} + R_{SRH}$), where R_{SRH} is the Shockley-Read-Hall model g/r rate [5], [6].

When defects or heavy-metal contaminations are induced by implantation processes, they are likely to be distributed near the metallurgical junction or at the Si/SiO_2 interface. As a mathematical model of locally generated deep-traps, we developed a three-dimensional point model (Fig. 2(a)), and used this model to analyze the leakage current including the deep-trap-assisted component. The total number, N_T, of deep traps is obtained from

$$N_T = \int N_{DD} dV = \sum N_{DD} \Delta x \Delta y \Delta z. \quad (6)$$

We also developed a belt-like distribution model (Fig. 2(b)). In this model, the current can be calculated from a two-dimensional simulation of a cross-section of the device.

In the next section, the reverse-biased junction current is precisely analyzed using two- and three-dimensional device simulations, focusing on the spatial location/distribution of deep traps and on the quantity of traps.

3. Results and discussion

Assuming spatially localized donor-type deep-traps, we

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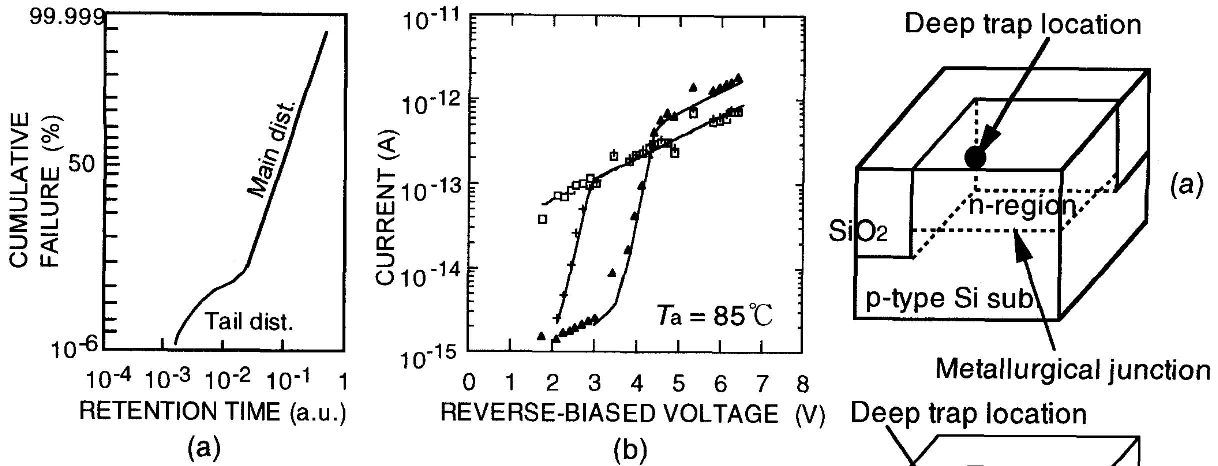

Fig. 1 Cumulative failure distribution of retention time (a) and current-voltage characteristics (b) observed in small pn junctions (after Ogasawara *et al.*, [1])

Fig. 2 Illustration of a pn junction and the spatially localized deep-trap model. (a) Three-dimensional point model. (b) Two-dimensional belt model.

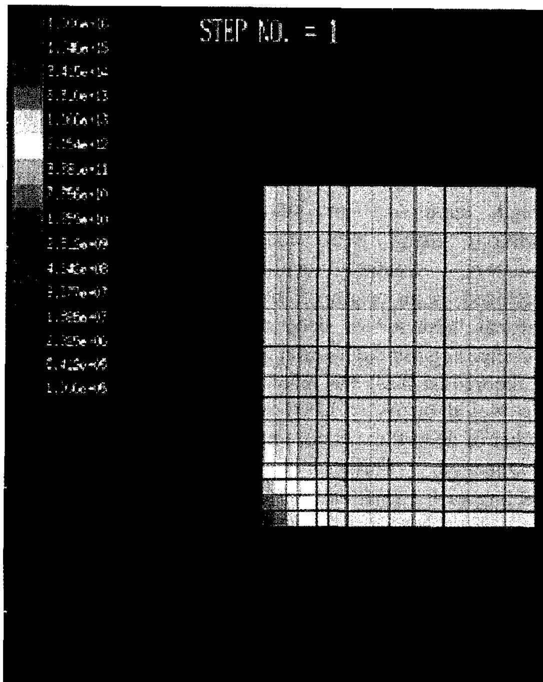

Fig. 3 Carrier distribution analyzed by three-dimensional simulation. The result is given in a cross-section which includes the deep-traps and is parallel to the device surface. The carrier density is represented by colors.

carried out three-dimensional simulations. Here, a point defect was assumed to be located at the corner of the pn junction, as shown in Fig. 2(a). When a high reverse-biased voltage is applied through the pn junction, the depletion layer expands and then includes the deep-trap center. This causes carriers to be generated from the trap-located portion, as shown in Fig. 3, due to the negative value of R_{DD} when $np << n_i^2$ in the depletion region.

We inferred that the high-level saturation current shown in Fig. 1(b) is caused by deep-trap-assisted carrier-generation. The high level current was evaluated as a function of the capture rate C with fixed N_{DD} (Fig. 4) because the g/r rate R_{DD} is linearly dependent on the $C \times N_{DD}$ product if we assume $C_n = C_p$. The reverse-biased current was calculated for the two device structures shown in Fig. 4, where the total number of deep traps was set to 50 at one mesh point and the energy level E_t was assumed to be located at the middle of the energy gap.

A current of less than 10^{-13} A is linearly dependent on the magnitude of the capture rate and is independent of the trap-generated location, whether at the corner or the center portion along the Si/SiO_2 interface. However, a current on the order of 10^{-13} A depends on the trap-generated location due to the influence of the spreading-resistance.

Comparing the calculated results with experimental data (the shaded area of Fig. 4), we estimated the capture rate was 10^{-6} cm^3/s or less. If deep traps are induced by heavy-metal contamination, the capture rate is in a range between 10^{-9} - 10^{-7} cm^3/s [7], depending on the impurity atoms. As a first-order approximation, we roughly estimated that the capture rate would be 10^{-8} cm^3/s. If so, the estimated total number of traps would be around 10^3.

That is, the high-level saturation-current can be caused by 1,000 locally generated deep-traps, which is not unrealistic for heavy-metal contamination, for example, that of Fe ions.

In contrast, the low-level current appears to result from bulk g/r centers or interface traps. However, the current calculated from the bulk g/r model, R_{SRH}, is small compared with the experimental data. Further, it is experimentally known that the magnitude of the reverse-biased current depends on the junction perimeter, rather than the junction area size. Thus, we analyzed the low-level current assuming interface traps as shown in the insert of Fig. 5. The analyzed current is plotted as a function of the recombination velocity s_r, where $s_r = C \times N_I$ with N_I being the interface trap density. For simplicity, the velocities for electrons and holes were assumed to be equal in the simulation. Comparing our calculated results with the experimental data, we estimated the recombination velocity was about 100 cm/s.

Under reversed-biased conditions, the surface/interface generation velocity s_g is given by

$$s_g = \frac{s_n s_p}{s_n \exp(E_t - E_i) + s_p \exp(E_i - E_t)}, \quad (7)$$

where s_n and s_p are the recombination velocities for electrons and holes [8]. The magnitudes of s_g and s_r, respectively, have been reported to be in ranges of 0.1-1 cm/s and 100-1000 cm/s for a well passivated Si/SiO_2 interface [8], although the generation/recombination velocity is dependent on the surface state.

In the present simulation, a discrete energy level in the band gap was assumed and E_t was set to the center of the gap, although the surface state has a continuous energy level throughout the gap. In fact, the energy level E_t, which contributes to the current flowing through the pn junctions, is limited within a narrow range near the center of the band gap. For example, assuming a discrete energy level, we analyzed the magnitude of the current as a function of E_t. Here, the $C \times N_I$ product s_r was fixed at 100 cm/s. Our calculated results are shown in Fig. 6. The current level decreased exponentially when E_t deviated from the center of the band gap. If E_t deviated from the mid-point of the gap by about 0.1 eV, the estimated magnitude of s_g was about 1 cm/s, which is comparable to the experimentally obtained data. Thus, by using single-level modeling, the current level can be quantitatively predicted with reasonable accuracy.

Finally, we analyzed the current-voltage characteristics and compared our calculated results to experimental data (Fig. 7). In our simulation, 1,000 deep traps were generated along the dark area in the insert of Fig. 7, rather than at one spatial-point as in Fig. 2(a); if 1,000 traps were generated at one point, the trap density would be extremely high. The capture rate for both electrons and holes was assumed to be 10^{-8} cm^3/s and the energy level E_t was set at mid-gap. Interface traps in the hatched areas were modeled and characterized by a 100-cm/s recombination-velocity.

The steep increase in current and the saturation were clearly demonstrated and the calculated results agreed well with the experimental results. When deep traps are spatially localized near the metallurgical junction, the steep increase in current with an increasing reverse-bias can be explained as follows: when a high reverse bias puts the trap-generated location in the depletion layer, the deep traps change the electrical state from non-active to active. Therefore, the critical voltage V_c, above which the current steeply increases, depends on the deep-trap location. In our present analysis, calculations were carried out assuming a 0.01-μm location-difference for the deep trap center represented by the dark area in the insert of Fig. 7. This difference in the trap-location induced about a 1-V difference in the critical voltage V_c. This deep-trap model, on the whole, can qualitatively and quantitatively demonstrate the anomalous behavior observed in small-dimension pn junctions, including fluctuations in V_c.

4. Conclusions

When pn junctions have been made extremely small and integrated with an ultra-high density, unexpected high-level currents have been observed at a low appearance probability. We have analyzed the current flowing through small-size pn junctions under reverse-biased conditions using two- and three-dimensional device simulators. Spatially localized deep trap models were introduced as an origin of the high-level current, and the electrical behavior of deep traps was precisely studied. By comparing our calculation results with experimental data, this theoretical study has indicated that the quantity of deep-traps would be N_T = 1,000 with $C = 10^{-8}$ cm^3/s. This number of deep-traps is not unrealistic, but is extremely low for detection. Further research, especially into ways of detecting such a small number of deep-traps, is required.

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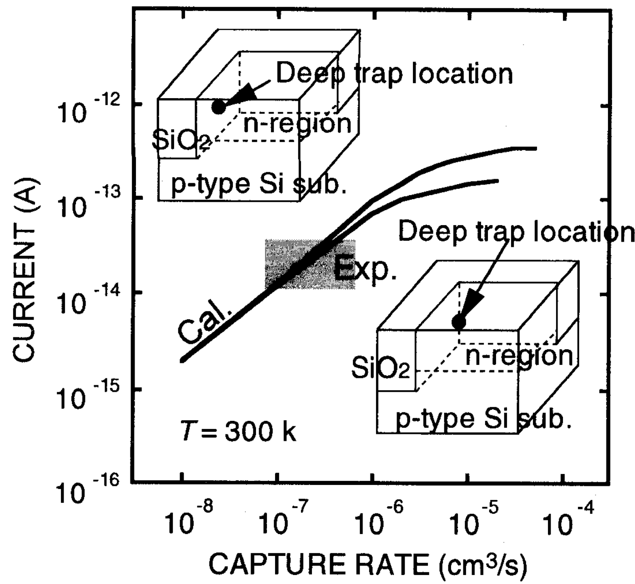

Fig. 4 High-level saturation current analysis. Three-dimensional simulation results and measured current levels are denoted by the solid line and the shaded area, respectively. Here, the junction area size is assumed to be (0.5 μm) x (0.5 μm).

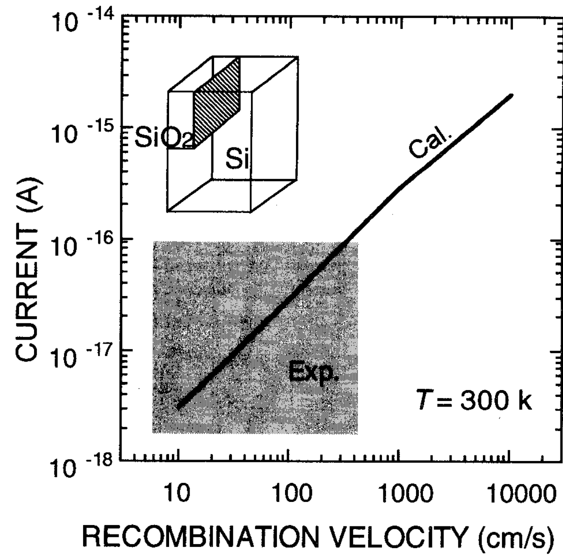

Fig. 5 Low-level current analysis. Assuming interface traps in the hatched area of the insert, the current was analyzed as a function of recombination velocity by two-dimensional simulation. Experimental current levels are indicated by the shaded area.

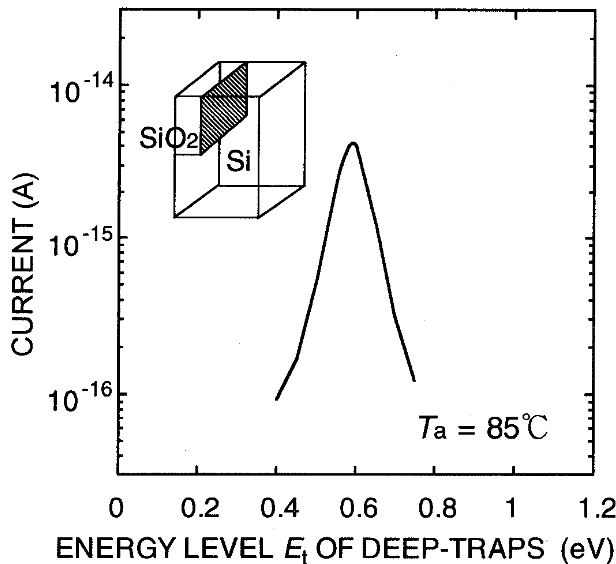

Fig. 6 The reverse-biased pn-junction current as a function of the energy-level of Si/SiO_2 interface traps located in the hatched area. Here, the junction area is assumed to be (0.5 μm) x (0.5 μm) and the recombination velocity is assumed to be 100 cm/s.

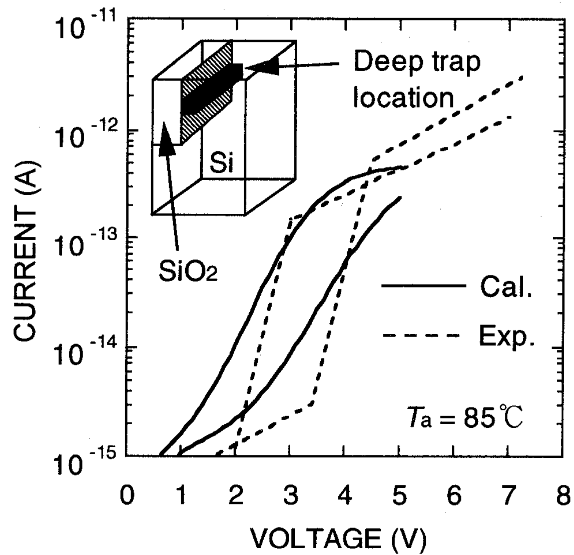

Fig. 7 Current-voltage characteristics. Two-dimensional simulation results and measured data are denoted by the solid and broken lines, respectively. In the simulation, 1,000 acceptor-type deep-traps were generated along the dark area in the insert and interface traps characterized by a 100-cm/s recombination velocity were assumed to lie in the hatched area.